An asymmetrical bulk-modified composite MOS transistor with enhanced linearity

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Abstract—In this work, an asymmetrical bulk-linearized composite MOSFET is presented, with an enhanced linear range and an equivalent saturation voltage of up to several hundred mV even in weak inversion, allowing to implement large MOS resistors. Some preliminary measurements are presented, as well as 150MΩ and 200MΩ equivalent resistors simulations, with a linear range up to 1.5V. A low frequency, 40dB gain, fully integrated cardiac sensing channel filter/amplifier is also shown. Taking advantage of the proposed technique, the circuit consumes only 25nA of supply current.

Index Terms— analog integrated circuits, CMOS, linearization techniques, analog filters, MOS resistor.

I. INTRODUCTION

BULK degeneration completes the three basic techniques used for linearization of the MOS transistor, the two other are source and gate degeneration [1,2,3]. Yet, bulk linearization of a MOS differential pair was only introduced in 2007 [4] (and further developed in [5,6]) where an increasing compensating voltage is applied to the bulks of a differential pair, thus decreasing the transconductance and increasing the linear range. The technique is proposed in [4] including simulations, a measured transconductor and a nano-power G$_m$-C filter are presented in [5], while a high frequency OTA is presented in [6] including measurements of the HD$_3$ distortion optimum already simulated in [4,5]. A similar concept was introduced for a single MOSFET operating in the triode region in [7], applying a compensating voltage to the bulk in order to widen the linear region. The idea is retaken in this work: firstly, a new asymmetrical bulk-modified transistor is presented, and novel circuits are proposed to implement practical MOS pseudo-resistors based in this structure up to hundreds MΩ. Finally, a G = 200, 1.5V$_{PP}$ output bandpass amplifier for cardiac activity detection in pacemakers is presented, which consumes only 25 nA thanks to the use of bulk-linearized pseudo-resistors.

II. AN ASYMMETRICAL BULK-MODIFIED MOS COMPOSITE TRANSISTOR WITH ENHANCED LINEARITY

In the so-called MOS resistor, the transistor is operated at the beginning of the triode region, where the drain-source voltage

V_{DS} is small, with fixed bulk and gate voltages. The drain current I_D should be proportional to V_{DS} but, due to the non-linear nature of the MOS itself, the linear range is severely limited as in Fig. 1a. The basic idea of using the bulk to extend the linear region is shown in Fig. 1b, where the bulk is connected to the drain of M$_1$ (V_{GS} is fixed). The slope $(r_{MOS})^{-1}$ of $I_D(V_{DS})$ can be calculated with a small signal analysis:

$$i_D = (g_{mb} + g_{md}) \cdot v_{ds} \quad \Rightarrow \quad r_{MOS} = (g_{mb} + g_{md})^{-1} \quad (1)$$

where g_{mb}, g_{md}, are the bulk and drain transconductances respectively. The MOS equivalent resistance r_{MOS} is not constant because both g_{mb}, g_{md}, depend on V_{DS}. At $V_{DS} = 0$V, $g_{mb} = 0$, and the drain transconductance is a given value $g_{md} = g_{mdo}$; when V_{DS} increases, g_{md} decreases, becoming virtually 0 as M$_1$ saturates, but g_{mb} increases thus the bulk modulates I_D. For a MOS behaving as a resistor, $r_{MOS}(V_{DS})$ in (1) should be constant (g_{mb} increase should compensate g_{md} decay). While for the large signal MOS it is not straightforward to develop an analytic expression of (1), the design space can be explored with a SPICE simulator; the result for a long transistor with $W_1/L_1 = 1\mu m/10\mu m$ is shown in Fig.1b ($V_{GS} \approx V_T$) with a quasi-linear range up to 400mV when the bulk-source diode starts conducting a significant current. In effect, the problem with the circuit in Fig. 1b is the directly biased diode triggering the drain current, and eventually latchup as V_{DS} increases. To overcome this problem and to further enhance the linear range, the proposed bulk-modified composite transistor is shown at the top of Fig.2: M$_1$ has been split in two series transistors, M$_{1a}$ sized $(W/L)_{1a}$, and M$_{1b}$ sized $(W/L)_{1b}$, and the bulk voltage V_B is generated from the M$_{1a}$-M$_{1b}$ MOS divider itself. A reference current and a diode-connected transistor M$_{Bias}$ = M$_{1b}$ are used to set V_G. Moreover, M$_{1a}$-M$_{1b}$ can be considered as an equivalent 3-terminal composite MOS M$_{eq}$ that saturates for a large V$_{Sat\_eq}$ > 400mV as depicted in Fig.2. The linear region is greatly extended, the best linearity results were obtained for $(W/L)_{1a} \gg (W/L)_{1b}$ thus the composite transistor will be asymmetrical. When V_{DS} increases, as $(W/L)_{1a} \gg (W/L)_{1b}$, the voltage drop in M$_{1a}$ is small so M$_{1b}$ rapidly saturates, while M$_{1a}$ remains in the
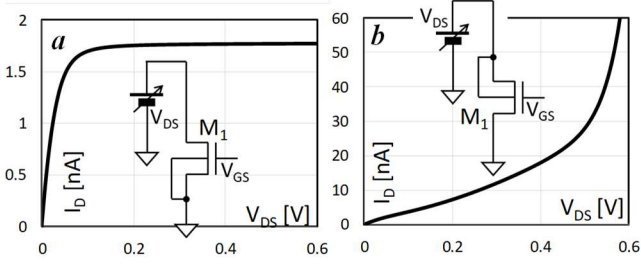
Fig. 1. **a)** Simulated $I_D(V_{DS})$ for a standard NMOS; **b)** a very basic bulk linearized MOS; $W/L = 1\mu m/10\mu m$, V_{GS} close to threshold voltage V_T.
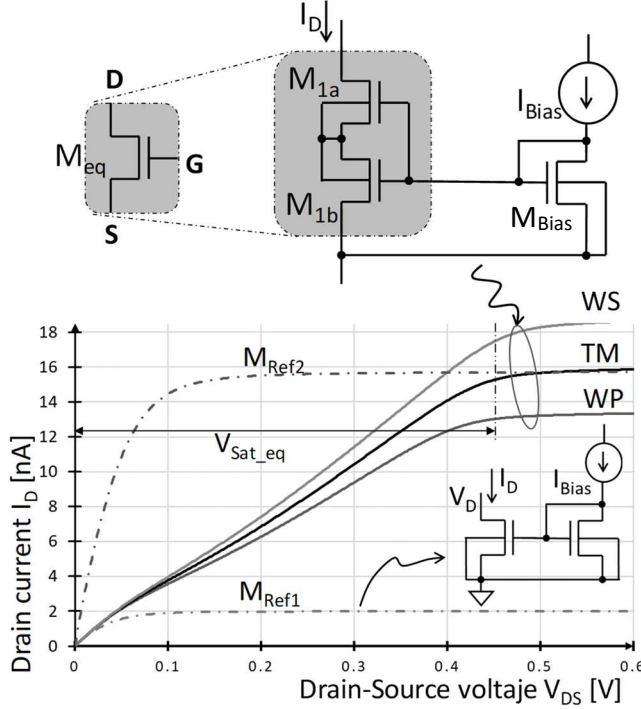

Fig. 2. The proposed asymmetrical bulk-modified MOS. M_{eq} on top, and simulated $I_D(V_{DS})$ transfer (straight lines) for typical, worst-slow, worst-power foundry models (TM, WP, WS). Two reference transistors (dash-dot lines) are included to compare the impact of linearization. Note the equivalent V_{Sat_eq} above 400mV.
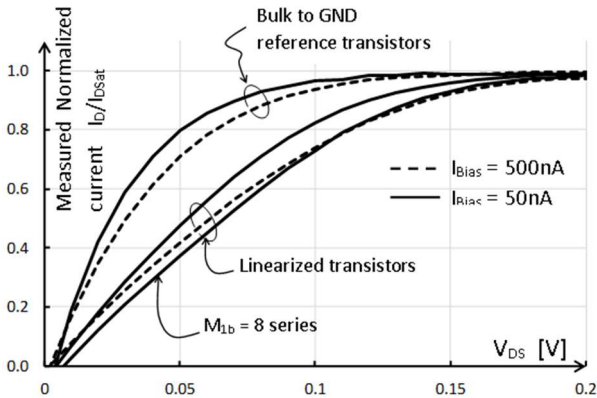

Fig. 3 Measured bulk-linearized MOS using discrete transistors.

linear region.   But as M_{1a} source V_{S1a} (connected to V_B) increases, V_{GS1a} decreases to such an extent that, at certain point, I_D is close to the saturation current of M_{1a}. From this point on, the voltage drop in M_{1a} increases rapidly, and M_{eq} transistor reaches saturation resembling a cascode. The simulations in Fig. 1, 2, 4, 5, correspond to a 0.6μm technology with $V_{TN} \approx 1V$;

in Fig.2 $(W/L)_{1a} = 10\mu m/1\mu m$, $(W/L)_{1b} = (W/L)_{Bias} = 1\mu m/40\mu m$. Preliminary measurements for bulk-linearized MOSFETs using ALD1106 quad discrete transistors in the configuration of Fig.2 are shown in Fig. 3. M_{1a}, and M_{1b} of Fig. 2 were implemented with 4-parallel and 4(8)-series transistors respectively. The measured linearization effect is remarkable, but quite limited in comparison to Fig. 2 because of the limited aspect ratio of these discrete MOSFETs. Notice that the M_{eq} composite transistor can be effectively considered as a single unit transistor. In Fig. 4 several $I_D(V_{DS})$ curves, the equivalent saturation current $I_{Sat}(V_{GS})$, and the equivalent $[g_m/I_D]$ ratio, are shown for a composite M_{eq} (continuous line) and a single reference transistor M_{Ref} (dash-dot line). M_{eq} can be utilized to implement operative current mirrors and differential pairs, but are of little practical interest because of the large V_{Sat_eq}. On the other hand, M_{eq} can be exploited to efficiently implement MOS pseudo resistors with enhanced linearity in a reduced die area.
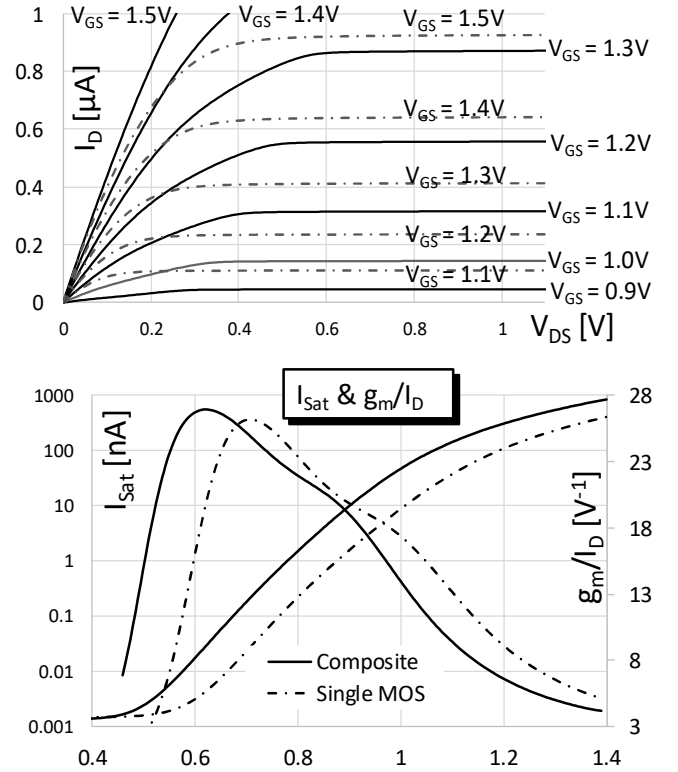

Fig. 4. Simulated $I_D(V_{DS})$ for different V_{GS} values (top plot), saturation current I_{Sat} and g_m/I_D ratio (bottom plot); for a bulk-modified composite transistor (continuous line) $W_a/L_a = 10\mu m/0.6\mu m$, $W_b/L_b = 0.6\mu m/10\mu m$, and a standard NMOS (dash-dot line) $M_{Ref} = 0.6\mu m/10\mu m$.

III. HIGH VALUE RESISTORS USING COMPOSITE TRANSISTORS

Very large pseudo-resistors using MOSFETs can be implemented therefore by stacking successive stages like the one in Fig. 2. Firstly, three blocks are connected in series as shown in Fig. 5 to implement a resistor close to $R_{MOS} \approx 200M\Omega$ with a quasi-linear range of almost 1V. The transistors are sized $(W/L)_a = 10\mu m/0.6\mu m$, $(W/L)_b = (W/L)_{Bias} = 0.6\mu m/60\mu m$; the 0.6nA and 1nA bias currents are implemented with PMOS current mirrors (not shown) and were adjusted to fine tune the

linearity. The addition of the bias currents in Fig. 5 makes the equivalent drain and source currents to be different: $I_A \neq I_B$, and thus shifts the $I_A(V_{AB})$ curve (to restore $I_A = I_B$, properly matched sink currents can be added at $V_{G1,G2,G3}$ gate nodes). Using this circuit to emulate a resistor has, nonetheless, the major drawback of requiring $V_{AB} > 0$, which seriously limits the range of possible applications. A solution is given in Fig. 6 where two blocks M_{up} and M_{low} like the one in Fig. 2, are connected in series in opposite direction and sharing the gate $((W/L)_a = (W/L)_c$, $(W/L)_b = (W/L)_d = (W/L)_{Bias}$. Since V_{GS} for the lower composite transistor M_{low} is higher, it practically does not affect I_D. The circuit is symmetrical thus the $I_D(V_{DS})$ is so, as depicted in the plot of Fig.6 corresponding to preliminary measurements using ALD1106 quad discrete transistors. Just as in Fig.3, the measured linearization effect is quite limited due to the aspect ratio of the discrete MOSFETs. But the results are amazing in Fig.7 where very different aspect ratios for the transistors were simulated, for two blocks analogous to the one in Fig. 6 connected in series, using PMOS transistors in a 0.18μm CMOS technology. A 150MΩ resistor is shown, with approximately 1.5V linear range, and consuming only 2nA current to bias the gates; the combined effect of the opposite stacked blocks also helps to compensate slight $r_{MOS}(V_{DS})$ variations in (1) that can be observed in Fig.2 for a V_{DS} small (before M_{1b} saturates). In Fig.7 sink bias currents are used to set M_{1i} gate voltage, and matched source currents are included for the sake of symmetry (to make $I_A = I_B$ again). The linear range to current consumption trade-off, is better than any other reported small transconductance OTA (see [5] for a survey).

IV. A 40 nA CARDIAC SENSE CHANNEL FOR IMPLANTABLE PACEMAKERS USING BULK-LINEARIZED MOS RESISTORS

A practical utilization of the linearized 147MΩ MOS resistor in Fig.7 is shown in Fig. 8, where a nano-power filter-amplifier for biomedical applications is presented. On the right side of the picture the G_m-R-C filter is shown while transistor-level
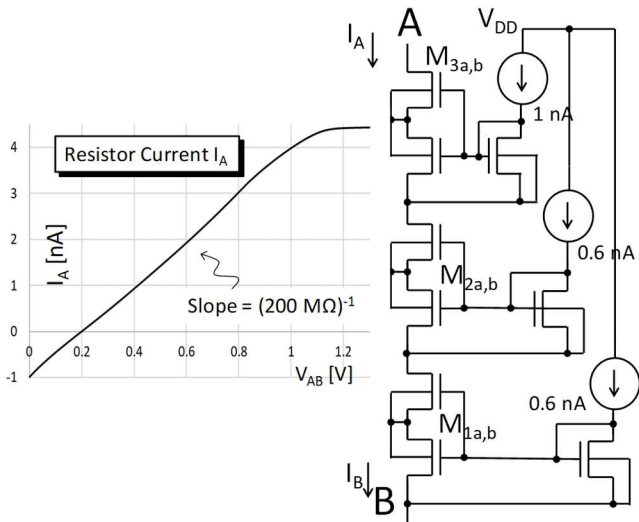
schematics for G_{m1}-G_{m1}' OTA are shown on the left. The idea was to substitute the very low transconductance linear OTAs that consume current in a G_m-C filter [5], by MOS resistors. In the proposed filter G_{m1}-G_{m1}' form a dual differential input transconductor with G_{m1} =125nS, G_{m1}' =38nS. The transconductor G_{m2} is utilized as an operational amplifier implementing an ideal integrator with C_2. Assuming a virtual V_{Ref} at the positive input of G_{m2}, G_{m1}-R_1-C_1 form a low-pass gain stage, and R_1-G_{m2}-C_2 act as an integrator:

$$V_{o2} = \int V_{Out}(t)/(C_2 \cdot R_1) \cdot dt \qquad (2)$$

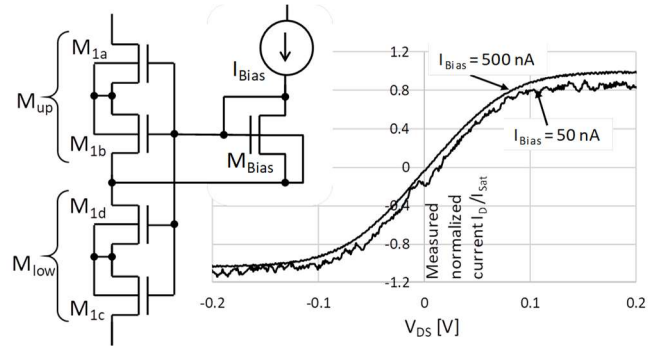Thus, it acts as a DC cancellation loop. In the filter $C_1 = 5pF$,

Fig. 6. Proposed circuit block to implement direct-reverse MOS resistors, and measured results using discrete transistors. For the plot, $M_{1a,c}$ and $M_{1b,d}$, were implemented with 4-parallel and 4-series unitary transistors respectively (each unitary transistor is ¼ ALD1106).
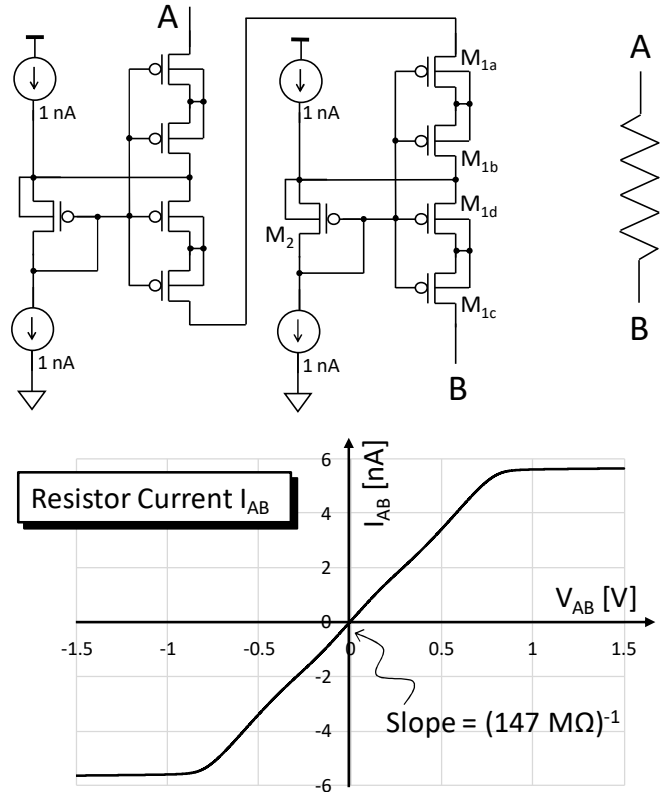
Fig. 7. Two double-sided linearized PMOS forming a ≈150MΩ equivalent resistor; $W_{a,c}/L_{a,c}$ = 10μm/0.4μm, $W_{b,d}/L_{b,d}$ = 0.6μm/40μm. Simulated results on the bottom.

Fig. 5. Three stacked bulk-linearized MOS form a 200MΩ equivalent resistor; W_a/L_a = 10μm/0.4μm, W_b/L_b = 0.6μm/40μm, simulated results on the left.
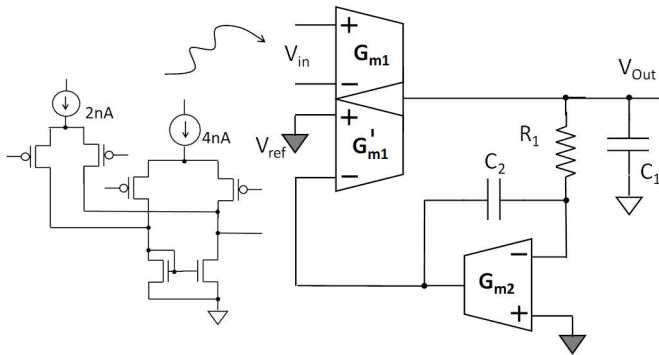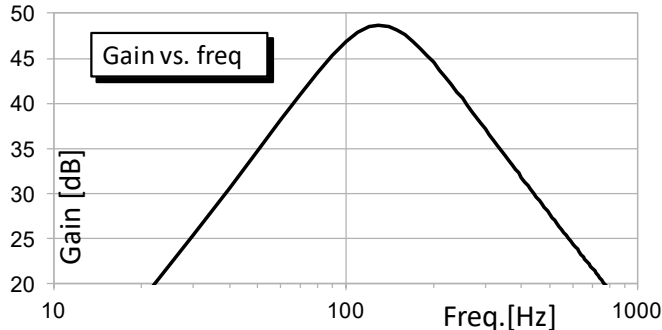
Fig. 8. The proposed G_m-R-C filter-amplifier .

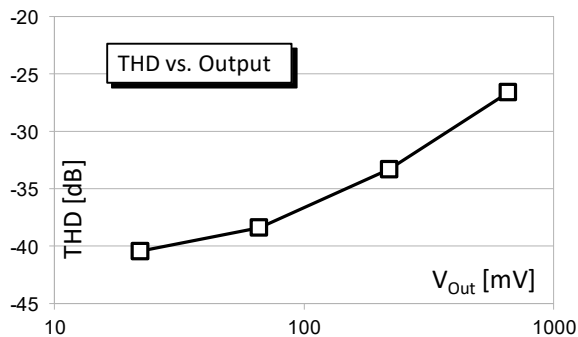Fig. 9. Simulated AC transfer function of a two stage, 40 dB/dec, filter for cardiac sensing.

Fig. 9. Simulated output THD@130Hz of the filter

$C_2 = 4$pF, and $G_{m2} \approx 1$nS is a symmetrical OTA with a 2nA bias current, and 32:1 series-parallel current division to the output as proposed in [8] to achieve a very low transconductance. The filter of Fig.8 is intended to amplify cardiac signals in an implantable pacemaker for natural heart beat detection. Cardiac sensing is a well-known application [9, 10]; the objective is to amplify 100μV – 10mV input signals and bandpass filter them around 70Hz-200Hz. A detailed description of the complete cardiac sensing signal processing chain (amplifier-filter + comparator, offset compensation, etc.) is omitted in this work for the sake of simplicity. For the minimum signal, the gain of the filter in Fig.9 is not enough, and thus two series stages need be employed with a total gain $G_{Tot} = 49$dB, and 40db/dec decay to eliminate noise out of the band of interest. For larger cardiac signals, it is easy to reduce the gain altering the R_1 biasing in Fig.7. In Fig.9, and Fig. 10, the simulated transfer function of the 2-stage filter, and the simulated output total harmonic distortion (THD) are shown. The circuit was simulated for V_{DD} in the range from 1.8V to 3.3 V in a 0.18μm technology and

consumes only 25nA in supply current. The THD is adequate for biomedical applications and is mostly the result of the 2nd harmonic effect.

V. CONCLUSIONS

In this work a bulk-linearization technique was presented, to enhance the linearity of the MOS transistor behaving as a resistor, using two series MOSFETs with the bulk connected to the midpoint. If properly designed, the resulting composite structure is linear up to an equivalent saturation voltage of several hundred mV. This asymmetrical bulk-modified composite MOS can be considered as a new transistor, with slightly degraded characteristics but enhanced linearity. Simulations and preliminary measurements using discrete transistors were presented. A 200MΩ 1V-linear equivalent resistor, and a 150MΩ 1.5V linear resistor were simulated stacking series linearized MOSFETs. For the latter, a technique was developed that allows to connect the equivalent resistor in both senses of the current flow. Finally, a biomedical circuit application example featuring a 25nA supply current, 49dB gain, 40dB/dec filter for cardiac signal detection was presented, using this technique to reduce the power consumption to a minimum in comparison to previously reported equivalent blocks. The proposed amplifier can substitute pure G_m-C, continuous time, or SC filter stages in [5, 9, 10] with a remarkable reduction of both supply current and supply voltage.

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