Analog Integrated Circuits and Signal Processing (2021) 107:617–628
https://doi.org/10.1007/s10470-021-01827-w

CMOS level shifters from 0 to 18 V output

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Received: 28 June 2019 / Revised: 28 January 2021 / Accepted: 20 March 2021 / Published online: 3 April 2021

Abstract
A design methodology for level shifters voltage translators, where the output voltage ranges from 0 to 18 V, and the input voltage ranges from 2 to 5.5 V in a 0.6 µm CMOS-HV technology, is presented. This family of circuits have a special interest in the case of implantable medical devices where is common to handle previously unknown voltages either positive or negative, above or below the control logic supply V_{DD}. Two application examples are presented: a composite switch to control negative stimuli voltage pulses, and a multi-channel programmable charge-pump voltage multiplier, aimed at charging the output capacitors of an IMD.

Keywords Level shifter · HV-CMOS · Biomedical circuits

1 Introduction

Level shifters are essential circuit blocks in multi-supply voltage circuits and systems. A level shifter (LS) translates logic levels between two voltage domains for example {0, V_{DD}} to {V_L, V_H}; but in most of cases the designers refer to level shifters as circuits translating at high speed and without static power consumption from {0, V_{DD}} to {0, $V_H > V_{DD}$} like in Fig. 1, where a classic standard level shifter schematic is shown [1–4]. V_H can be large, up to the maximum gate-source voltage V_{GSmax} that $M_{1\ldots6}$ can withstand (1–5 V in regular CMOS ICs); to translate to higher voltages domains current signalization and protection circuitry are necessary, which increase power consumption and circuit complexity. High voltage HV-CMOS transistors include a thick gate oxide for V_{GSmax} up to 18–20 V, and an extended drain to avoid large electric fields allowing elevated maximum drain to source voltages V_{DSmax}. In this work, a 0.6 µm HV-CMOS technology with 12.5 nm thin and 41 nm thick oxides allowing transistors with V_{GSmax} = 5.5 V and 18 V respectively was used. In Fig. 1, M1–M6 transistors are HV ones, the different symbol used indicates the thick oxide and the extended drain. LS can be useful in applications like communicating a low V_{DD} CPU to a 5 V peripheral, in HV displays, non-volatile memories, driving the gate of a high-side pass transistor in a switched converter, or in medical devices to implement tissue-stimuli delivery subsystems [4–8]. While in the first examples the design of a LS is simple because V_{DD} and V_H are fixed for each application, the latter examples become a challenging problem if V_H is a previously unknown voltage. In a biomedical circuit, V_H can be either 15 V, 5 V or 100 mV, depending on the device state and on the stimuli value programmed by the physician. This work proposes different circuit topologies to help the designer adapting the circuit in Fig. 1 to cover such a wide range for V_H. As an example application, a block diagram of a generic implantable medical device (IMD) is shown in Fig. 2, including electrodes to connect the tissue to voltage and/or current sources in the device through one or multiple pass-switches. The control logic supply voltage is assumed to be a low voltage V_{DD}, obtained from a medical grade battery, while the stimuli to deliver to the tissue in medical devices are either current or voltage pulses (or pulse trains) ranging from a few hundreds of mV to well over 15 V, or from a hundred µA to tens of mA. In this context, LS are necessary not only to open/close the switches and to directly deliver voltage pulses, but also to control the HV step-ups of the stimuli generator. The focus of this work will be the design of LS with the widest possible input and output voltage range, aimed at being a generic block for medical circuits. First, the design of a

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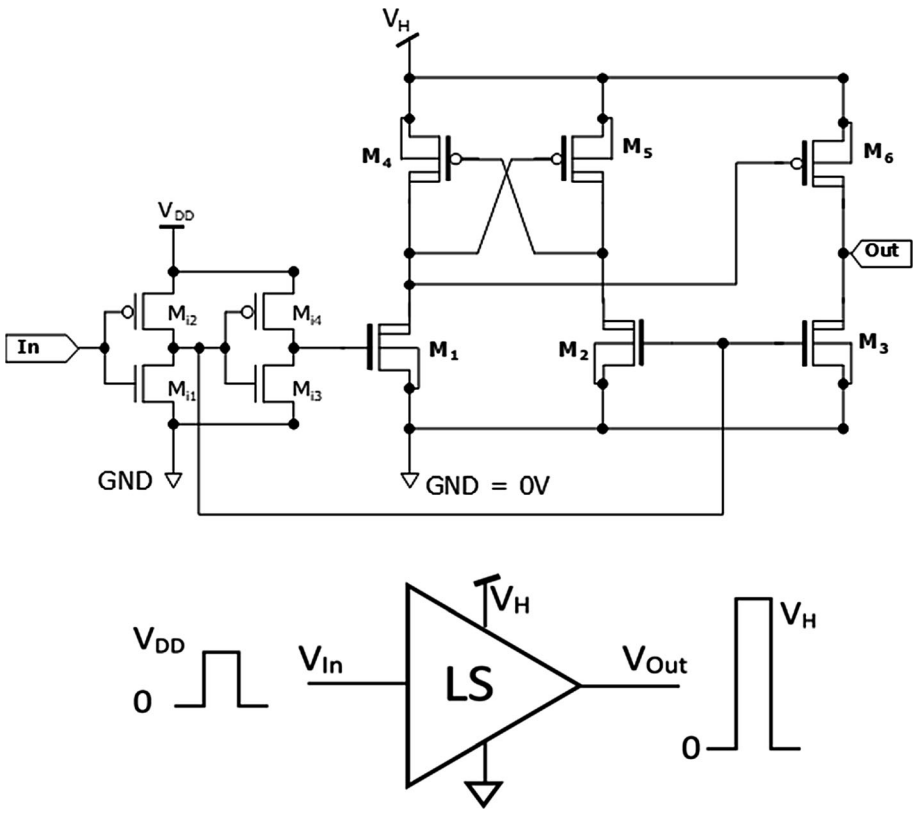


Fig. 1 A classic Level Shifter for $V_H > V_{DD}$. M_1–M_6 are HV transistors

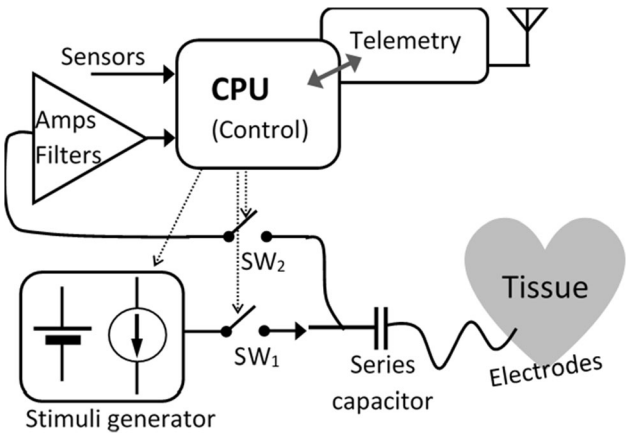


Fig. 2 General diagram of an IMD

full-range output LS is presented for V_H from 0 to 18 V. Then two application examples are presented: a composite switch to control negative voltage pulses, and a 0 to 16 V multi-channel programmable charge-pump multiplier, aimed at charging the output stimuli capacitors in IMDs.

2 Full range level shifters (FR-LS)

A full range LS was developed optimizing and modifying the circuit in Fig. 1; the challenge is to cover the full $0 < V_H < 18$ V voltage range, but since biomedical signals are of relatively low frequency the LS will not be optimized in terms of speed. V_{DD} is assumed to cover different usual types of batteries powering IMD's CPUs (2 V up to 5 V). The LS in Fig. 1 can be examined in two states, with the usual assumption $V_H > V_{DD}$;

- A "High" state when the input is set to V_{DD}, transistors $M_{1,5,6}$ are turned on, $M_{2,3,4}$ are turned off, thus the output goes to V_H.
- A "Low" state when the input is set to 0 V transistors $M_{2,3,4}$ are turned on, and $M_{1,5,6}$ are turned off, thus the output goes to 0 V.

Note the LS itself is formed by the input inverters and the HV MOS $M_{1,2,4,5}$ while M_3 and M_6 are just larger output transistors to drive the external load. At first glance, determining the transistor sizes is straight forward to minimize the occupied area: $M_{3,6}$ are of minimum length (L_{min} = 3 µm in the target HV-MOS) and wide enough to drive a given load at the output at the required frequency. The remaining HV transistors are all equal, minimum sized W_{min}/L_{min} = 10 µm/3 µm unless too huge $M_{3,6}$ are necessary. But V_H has a very wide operation range so three cases

will be examined in detail: V_H close to V_{DD}, V_H much smaller than V_{DD}, and V_H much larger than V_{DD}. In the left of Fig. 3, the simulated behavior of the circuit in Fig. 1 is shown for $V_{DD} = 2$ V and using the typical transistor model (TM) and the above transistor sizes. Note that this LS works properly only in the case of V_H close to V_{DD} thus either the transistor sizes, and/or the circuit topology need to be modified. On the right of Fig. 3, the measured results of a fabricated LS where $M_{1,2,4,5}$ transistors where carefully sized to improve its operation at a large V_H are shown. Transistors sizing procedure is described below.

The problem for $V_H >> V_{DD}$ can be observed when the LS changes from the "Low" to "High" state as M_1's gate changes from 0 to V_{DD} turning on the transistor. At this point M_1 is saturated because $V_{GS1} = V_{DD}$, $V_{DS1} \approx V_H$, much larger than its saturation voltage V_{DSsat1}. M_4 transistor starts in the linear zone because $V_{DS4} \approx 0$ V. The gate capacitance C_{G5} of M_5 is then discharged, until at some point the drain currents of M_1 and M_4 are equal. In a first approach, to guarantee that the LS is triggered, the intersection point of $I_{D4}(V_{D4})$ (1) and $I_{D1}(V_{D1})$ (2) must be for $|V_{DS4}| > |V_{TP}|$ (note $V_{D1} = V_{D4}$); if this condition is not met M_5 and M_6 will not turn on. If M_1 transistor is saturated and in Strong Inversion (SI), and M_4 transistor is in the linear region:

$$I_{D1} = \beta_1 \cdot \frac{(V_{GS1} - V_{TN})^2}{2} = \beta_1 \cdot \frac{(V_{DD} - V_{TN})^2}{2}, \quad (1)$$

$$I_{D4} = \beta_4 \cdot (V_{GS4} - V_{TP}) \cdot V_{DS4} = \beta_4 \cdot (V_H - |V_{TP}|) \cdot V_{DS4}. \quad (2)$$

where V_{TN}, V_{TP} are the threshold voltages, $\beta = \mu \cdot C'_{OX} \cdot \frac{W}{L}$. In this point M_2 is open and V_{DS4} is fixed just by the charge in the parasitic capacitance C_{G5} of M_5 gate. While $(|I_{D1}| - |I_{D4}|)$ is positive C_{G5} is discharged:

$$V_{G5}(t) = V_H - \frac{1}{C_5} \int (I_{D1} - I_{D4}) \cdot dt. \quad (3)$$

When $|V_{DS4}| = (V_H - V_{G5}) > |V_{TP}|$ is possible to assume that M_5 is turned on and the LS rapidly completes state change. But if solving (3) V_{G5} reaches a steady voltage such that $(V_H - V_{G5}) < |V_{TP}|$ where M_5, M_2 leakages are equal, the LS will not change state remaining in a stable condition (should be metastable in a proper LS). A complete analytical solution to (3) is complex, but a simpler criterion is to check if when $V_{DS4} = V_{TP}$, $I_{D1} > I_{D4}$; in this case the LS will always change state. A good trade-off for transistor sizing is to make the intersection point of M_1 and M_4 drain currents be at $V_{DS4} = V_{TP}$. Using (1), (2):

$$\frac{W_4/L_4}{W_1/L_1} = \frac{\mu_N}{2\mu_P} \cdot \frac{(V_{DD} - V_{TN})^2}{(V_H - |V_{TP}|) \cdot |V_{TP}|} \Rightarrow \frac{W_1}{W_4} \approx 6.6. \quad (4)$$

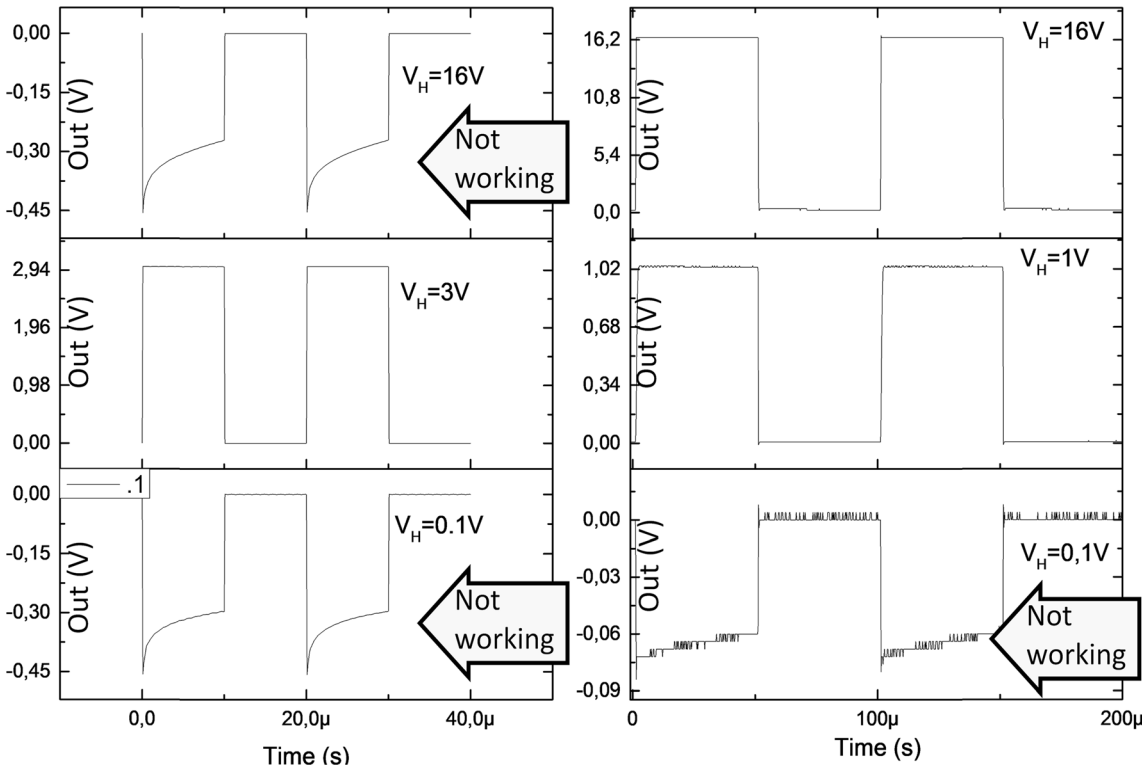


Fig. 3 Left: simulated output of the LS of Fig. 1, for a $V_{DD} = 2$ V, 50 kHz square wave input, classic approach. Right: measured output of the fabricated LS of Fig. 1, for a $V_{DD} = 2$ V, 10 kHz square wave input, $M_{1,2,4,5}$ sized using (4)

If all HV transistor lengths are L_{min} = 3 µm, and (4) is evaluated in the worst-case condition, V_{DD} = 2 V (end of life of a primary Lithium-Iodine pacemaker battery) and V_H = 18 V, the condition is that W_1/W_4 = 6.6. Note (4) is an overestimated criterion to guarantee LS transition which can be fine-tuned during simulations.

From Fig. 3, it is clear the LS does not properly work for a small V_H either. The reason is that $V_{GS} = V_H$ will not be high enough to turn on the PMOS HV transistors when required. Our proposed solution, shown in Fig. 4, is to connect NMOS HV transistors ($M_{7,8,9}$) in parallel with the HV-PMOS resembling a transmission gate configuration, but the gates of these HV-NMOS are controlled in the V_{DD} domain. When V_H is high, $M_{7,8,9}$ are transparent to the circuit as they are open, but they take the role of the PMOS when V_H is low. This new configuration of the LS, shown in Fig. 4, will be denoted as Full-Range Level Shifter (FR-LS). In Fig. 5 measurement results of a FR-LS at V_{H-} = 0.1 V, V_H = 1 V, V_H = 16 V show its correct operation in the complete full range. Summarizing, the following design methodology is proposed for a FR-LS. First determine the size of M_3 and M_6 according to the load. Then calculate the gate capacitances of these transistors, and determine the minimum width ($L = L_{min}$) of the $M_{1,2,4,5,-}$ transistors to drive this load at the required speed with V_H close to V_{DD}. Then increase $M_{1,2}$ width so that it is in compliance with (4). Finallly determine the size of M_7, M_8, M_9 for a worst case scenario with V_H = 0.1 V (or as low as required).

To validate the previous design, first a level shifter like the one in Fig. 1 was implemented and a FR-LS both following the previous design criteria. The selected values $W_{1,2}/L_{1,2}$ = 60 µm/3 µm, $W_{4,5}/L_{4,5}$ = 10 µm/3 µm result in a W_1/W_4 = 6 a bit smaller than the result in (4) so all corners were carefully simulated to guarantee it works in all cases. The output HV transistors $M_{3,6}$ are large enough

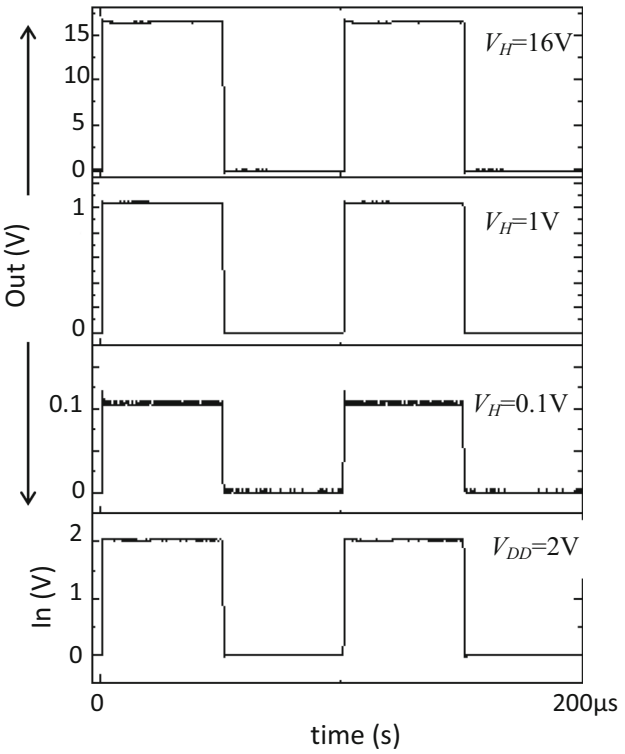


Fig. 5 Measured transient output of the fabricated FR-LS, for V_H = 0.1 V,1 V,16 V and a 10 kHz square wave input of V_{DD} = 2 V

to handle a 200pF @50KHz load, $W_{3,6}/L_{3,6}$ = 400 µm/3 µm. The measurement setup is shown in Fig. 6(a), where a microprocessor controls the triggering (IN signal) of both the LS and FR-LS, and V_H is swept with a digital power source. A 200pF load was connected at the outputs of both the LS and FR-LS and V_{DD} was fixed in a worst case value of 2 V. Transient measurements for the standard LS are shown in Fig. 3, it works properly for large V_H values but not for $V_H << V_{DD}$ since it lacks the configuration of Fig. 4. The transient measurements of the FR-LS of Fig. 4

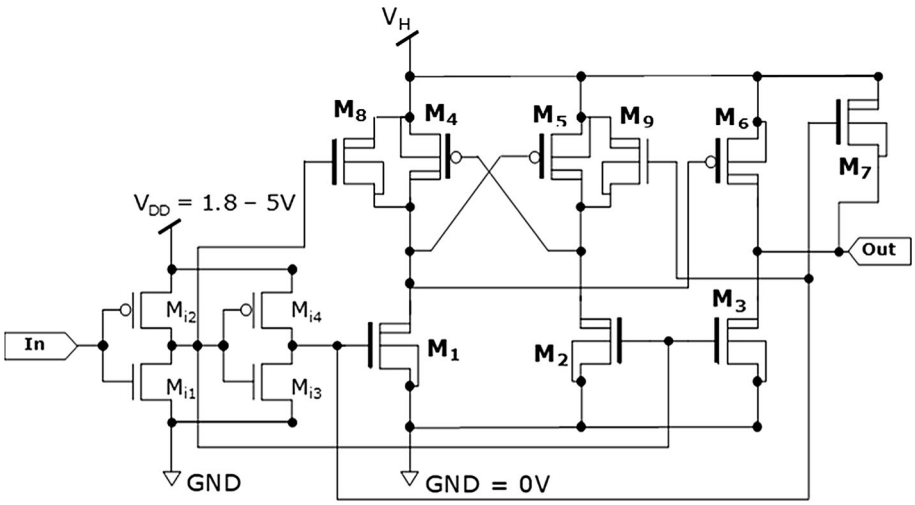


Fig. 4 Full range level shifter (FR-LS) circuit schematic

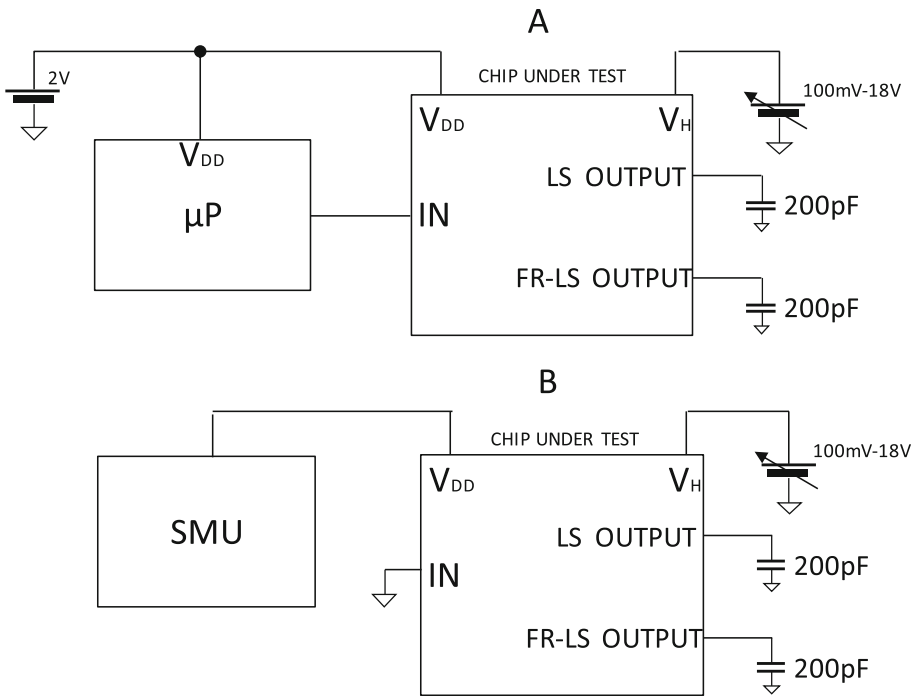


Fig. 6 LS measurement set up, **a** V_H range of operation, **b** Static power consumption

(W_7/L_7 = 400 µm/3 µm, $W_{8,9}/L_{8,9}$ = 10 µm/3 µm) are shown in Fig. 5, correctly working in the full range of V_H from 100 mV up to 18 V.

The delay for both LS and FR-LS were measured with a 200pF load, the results are shown in Fig. 7. In the case of the LS, the delay in the "0–1" transition is independent of V_{DD} but for the "1–0" transition, the delay varies with V_{DD} because the M_3 transistor on resistance (R_{ON}) is V_{DD} dependent. In the case of the FR-LS, the measured delay in both transitions ("0–1" and "1–0") varies with V_{DD} because either the PMOS or the NMOS transistors on resistance is important. Static power consumption was measured for both LS and FR-LS using a source measuring unit (SMU) to supply the V_{DD} and a fixed IN signal (Fig. 6(b) shows the measurement setup), in both cases the static power consumption was below 1nA.

To fully understand the operation of the FR-LS, in Fig. 8 a simulation is presented showing for a "0–1" transition with a 200pF load at the output, the percentage of the charge passing through both M_6 and M_7 in terms of V_H. Note for a low V_H almost all the current to charge the 200pF load goes through M_7 while for a large V_H goes through M_6. For V_H low ($V_H < 1$ V) the charge through M_6 is almost null, and at the end of the transition the output

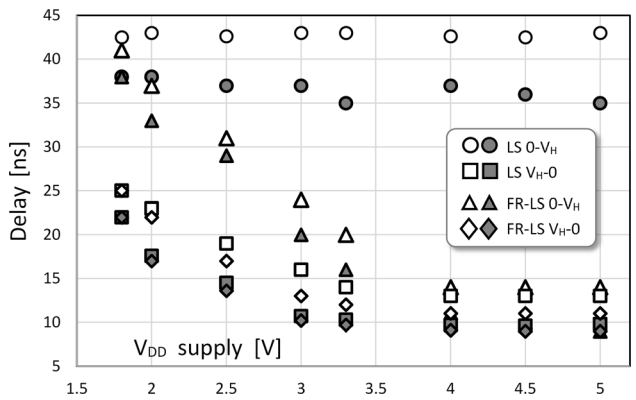


Fig. 7 Measured (grey symbols) and simulated (white symbols) delay of the LS and FR-LS, with a 200pF capacitive load at the output, V_H = 16 V and V_{DD} = 2 V

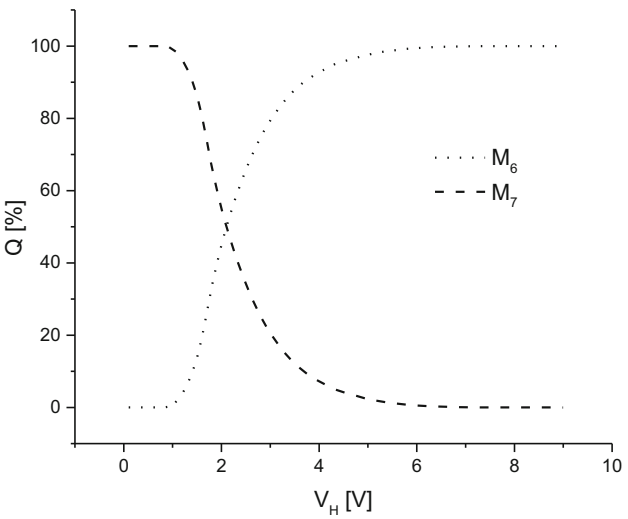


Fig. 8 Simulated percentage of the charge passing through both M_6 and M_7 in terms of V_H in a FR-LS, to charge a 200pF load in a "0–1" transition

voltage can be as low as 0 V; thus, in this situation M_6 never turns on but the Level Shifter properly operates thanks to M_7. For V_H around 2 V, the charge through of M_6 and M_7 is comparable, while for $V_H > 4$ V the effect of M_7 is negligible. M_7 transistor is placed so the Level Shifter operates for the lowest V_H range where M_6 does not turn on. Because of this reason the delay in Table 3 (measured at a large V_H) is almost the same for both.

M_7 size was not optimized for medium or large V_H values, instead it was sized by means of simulations using corners, to properly translate the logic '1' when $V_H < 1$ V, for a target load and worst-case delay. The result is a relatively large M_7 NMOS transistor in parallel with M_6. The FR-LS does not perform particularly better than the LS, apart from the fact that it covers the entire voltage range for V_H from 0 to 18 V, with a 40% penalty in the circuit area as shown in Table 3. Finally, it should be pointed a direct area comparison makes sense only between both versions of the LS with the same maximum V_H, but note in Table 3 the area is much higher for the level shifter in [9] achieving 300 V, and much smaller for the level shifter in [10] at 1.8 V. The maximum V_H voltage is the most relevant aspect to the occupied area, making necessary to utilize different technologies with different HV transistor types. Huge transistors are necessary to withstand 300 V like in [9] that are present in a few UHV technologies, while very small LV transistors may be enough in the case of [10]. Because of this reason the total area is orders-of-magnitude different while comparing the LS in [10], with those in this work, with the LS in [9], as highlighted in Table 3.

Finally, a negative level shifter (NLS) analogous to the one in Fig. 4 was also designed and fabricated, translating logic levels between $\{0, V_{DD}\}$ to $\{V_{SS}, V_{DD}\}$, where V_{SS} is a negative HV supply ($V_{SS} < V_{DD}$, $(V_{DD} - V_{SS}) < 18$ V). The NLS's schematic and microphotography are shown in Fig. 9 and Fig. 10 respectively. An NLS was implemented in a trench isolated HV-MOS technology on a Silicon on Insulator (SOI) wafer, that allows using negative voltages. In Table 1 transistors size for all three level shifters are presented, while in Table 2 a summary of the measured characteristics is presented. In Table 3 a comparison between this work and previously published LS [9, 10] is shown. A more accurate comparison is difficult as no other level shifter working for both ($V_H >> V_{DD}$) [9] and for ($V_H << V_{DD}$) [10] was published to the best of our knowledge.

Regarding the SOI process, it should be pointed that it is just a standard HV-CMOS fabricated on a SOI wafer including the ability to isolate different circuit blocks or transistors using oxide trenches. But the substrate layer is thick and true SOI MOSFETs cannot be implemented in this process. The manufacturer offers the same 0.6 µm process in both a standard wafer and the SOI wafer version. Dielectric SOI isolation may result in a reduced crosstalk, noise, and better EMC characteristics. In the case of medical devices, isolated NMOS transistors allow switching voltages below the die ground as shown in the next section, and is a valuable feature for the sake of reliability to avoid any latch up risk triggered by the output switches (e.g. in the case an unknown voltage is applied on critical PADs). But oxide trenches require to respect a relevant minimum distance to the transistors thus the die area increases a lot, particularly in the case of small and medium size MOSFETs. Because of this reason isolation feature was not utilized in the case of the voltage multiplier of Sect. 4, even though the circuit was implemented in the SOI version of the process. All the LS and FR-LS measurements including those in Table 3 were obtained using the standard 0.6 µm process, the NLS and composite switch in the next section where implemented in the SOI

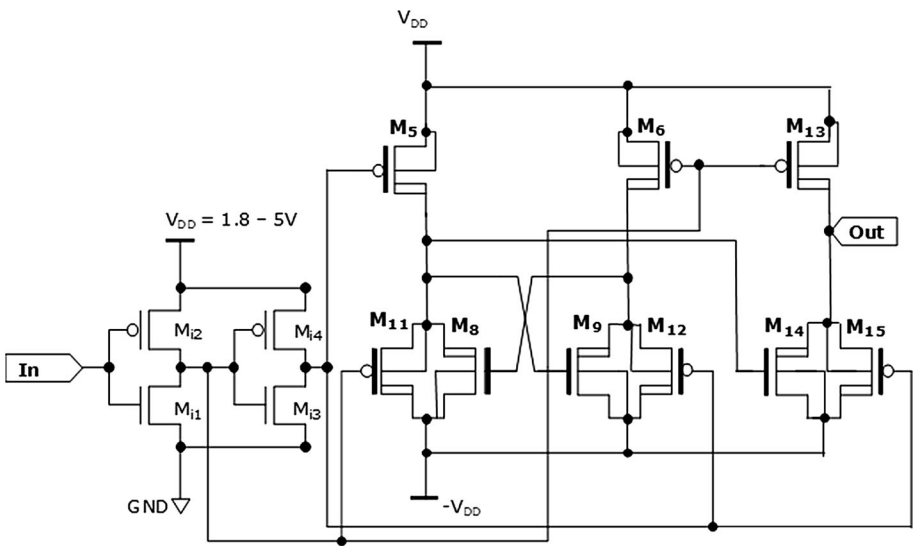


Fig. 9 Negative level shifter (NLS) schematic. $V_{SS} = -V_{DD}$ in the image

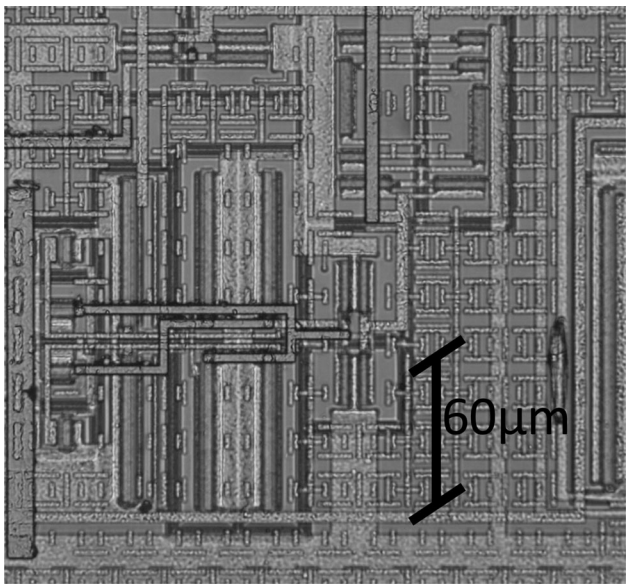


Fig. 10 Microphotography of the fabricated NLS

Table 1 Level shifters transistor sizes

Transistors	W/L (µm/ µm)
M_{i1-4}	20/3
$M_{1,2}$	60/3
$M_{3,6}$	400/3
$M_{4,5}$	10/3
M_7 (FR-LS)	400/3
$M_{8,9}$ (FR-LS)	10/3
$M_{5,6,13,14,15,16}$ (NLS)	60/3
$M_{8,9,11,12}$ (NLS)	10/3

process as necessary to deliver negative voltage pulses. Summarizing, there is no specific need to use a SOI wafer in the case of the proposed level shifters except for the NLS driving negative voltages, and as far as we could measure there were no observable differences between both versions. The SOI process was selected because of reliability, and to drive negative voltages like in Sect. 3 involving other circuit blocks that are not described in this work.

3 A composite switch for negative voltage pulses

A first application for the developed level shifters is shown in Fig. 11, were two NLS and two large NMOS transistors M_{S1}, M_{S2} sized 3000 µm/3 µm, are used to implement a composite switch, that may substitute SW_1 in Fig. 2, to deliver negative voltage stimuli pulses to a biological tissue. The configuration is analogous to that presented in [11] for pacemakers, including a C_{S1} = 5µF series safety capacitor, and a charge balance switch SW_2. A composite switch is necessary because the tissue voltage is unknown, thus is necessary to block current in both directions when not stimulating. To close SW_1 both NLS connect the gate voltages V_{GS1}, V_{GS2} to V_{DD}; to open SW_1 each NLS connect the gates V_{GS1}, V_{GS2} to M_{S1}, M_{S2} sources respectively. Connecting the gates to the sources helps to minimize crosstalk between multiple electrodes connected to the tissue because if SW_1 is open and a pulse is delivered through a different electrode connected to the tissue, the impact of the source-gate capacitance C_{GS1} is minimized, so the parasitic current through the electrode is negligible. The circuit was fabricated in the 0.6 µm HV-CMOS technology in the SOI wafer; M_{S1}, M_{S2} in Fig. 11 are dielectrically isolated MOSFETs as well as M_8, M_9, M_{14} in Fig. 9 (joint isolated). A measured 2 ms, − 14 V pulse, is also shown in Fig. 11, using a 500 Ω resistor to simulate tissue impedance according to the EN 45502-2-1 standard [12]. When the pulse starts, the tissue voltage V_P = − 14 V but the amplitude decays with time because C_{S1} and the electrode-tissue interface are charged at the same time. When the pulse finishes, SW_2 is closed for the charge balance to discharge C_{S1} and a real electrode's capacitance and to avoid any tissue damage [11, 13]. Also, in Fig. 12 simulation of a − 14 V pulse stimulation, using a 100 Ω, 1k Ω and 10 kΩ tissue impedance model is presented; no significant change in pulse maximum value is detected, this is due the proper design of transistors M_{s1} and M_{s2} of Fig. 11.

Table 2 Level shifters measurement results

Characteristic	LS	FR-LS
V_{DD} (V)	$5.5 > V_{DD} > 2$	$5.5 > V_{DD} > 2$
V_H (V)	$V_{DD} < V_H < 18$ V	$0 < V_H < 18$
Delay 0–V_H (V_H = 16 V, V_{DD} = 2–5 V, 200pF load) (ns)	43	45–10
Delay V_H–0 (V_H = 16 V, V_{DD} = 2–5 V, 200pF load) (ns)	25–10	22–10
Static current consumption (V_{DD} = 2–5 V)	< 1nA	< 1nA

Table 3 This work and previously published LS [9, 10] characteristics

Characteristic	LS (this work)	FR-LS (this work)	[9]	[10]
V_{DD} (V)	$5.5 > V_{DD} > 2$	$5.5 > V_{DD} > 2$	5	0.4
V_H (V)	$V_{DD} < V_H < 18$	$0 < V_H < 18$	$5 < V_H < 300$	$1.62 < V_H < 1.8$
Delay 0–V_H (ns)	43	45–10	12,000 (best case)	6.1
Delay V_H–0 (ns)	25–10	22–10	4700 (best case)	n.a
Static current consumption	< 1nA	< 1nA	620nA	0.23nA
Total area (μm^2)	3000	4200	124,000	35

Note the total area difference because the circuits are fabricated in different technologies to withstand very different output voltages V_H. A comparison makes sense only between both versions of the LS in this work, while the delay, area, power consumption, depend on the technology that is different in the two rightmost columns

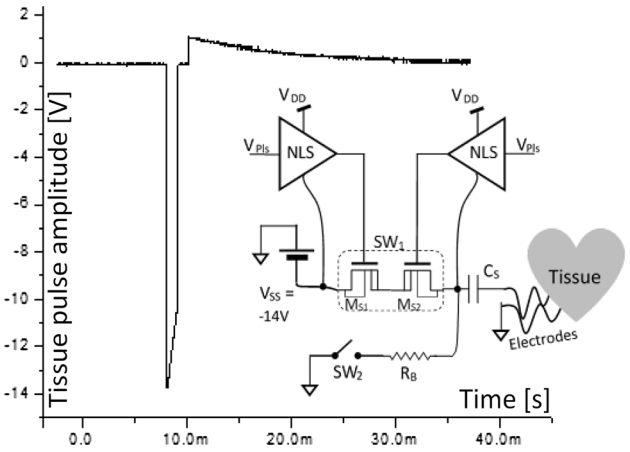


Fig. 11 A scheme of a composite switch and NLS drivers to delivery negative pulses to tissue, and measured − 14 V, 2 ms pulse. Charge balance also shown

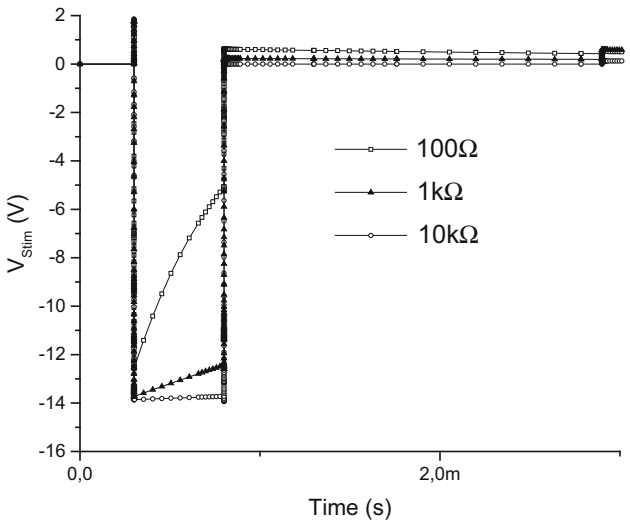


Fig. 12 Simulation of a − 14 V pulse stimulation, using a 100 Ω, 1k Ω and 10 kΩ tissue impedance model. Charge balance also shown

4 A fully programmable charge pump voltage converter for implantable medical devices

A high voltage generator is a necessary circuit block in most active IMDs, as regular stimuli pulses may be of 15 V or more. Charge pump voltage multiplier (VM) topology using external capacitors, is known to be preferred for pacemakers because of its efficiency at a minimum output current [5, 11, 14]. But while charge pumps are well known circuits, there is little detail available about how to switch voltages above V_{DD}. The basic VM topology used in this work is shown in Fig. 13, where multiple storage capacitors can be added to have multiple independent outputs. For a classic "3 × " voltage generator two pump capacitors C_{P1}, C_{P2}, are alternatively charged to the battery voltage V_{DD} (ϕ1 is the "charge phase") and then connected in series to the battery itself to achieve a $3 \bullet V_{DD}$ voltage. At this point the charge is transferred to an output storage capacitor C_{Sto} (ϕ2 is the "pump phase"); normally $C_{Sto} >> C_{P1,2}$ so no large output voltage steps are observed. A DC load can be connected in parallel to C_{Sto}, but in a pacemaker, for example, C_{Sto} is just charged up to a target value V_{Targ} ($0 < V_{Targ} < 3 \bullet V_{DD}$) and later discharged trough the tissue for a short time pulse when a stimulus is required. Other possible configuration of the same circuit are "2× " where only C_{P2} is periodically charged and later connected in series to the battery thus $V_{Targ} < 2 \bullet V_{DD}$; or "1× " where C_{P2} is periodically charged and used to transfer charge to C_{Sto} thus $V_{Targ} < V_{DD}$. While the 3× configuration is enough to select any V_{Targ}, to improve power efficiency the 3 configurations can be programmed in the proposed VM.

In a charge pump circuit, power efficiency η_P and charge efficiency η_Q can be defined as follows:

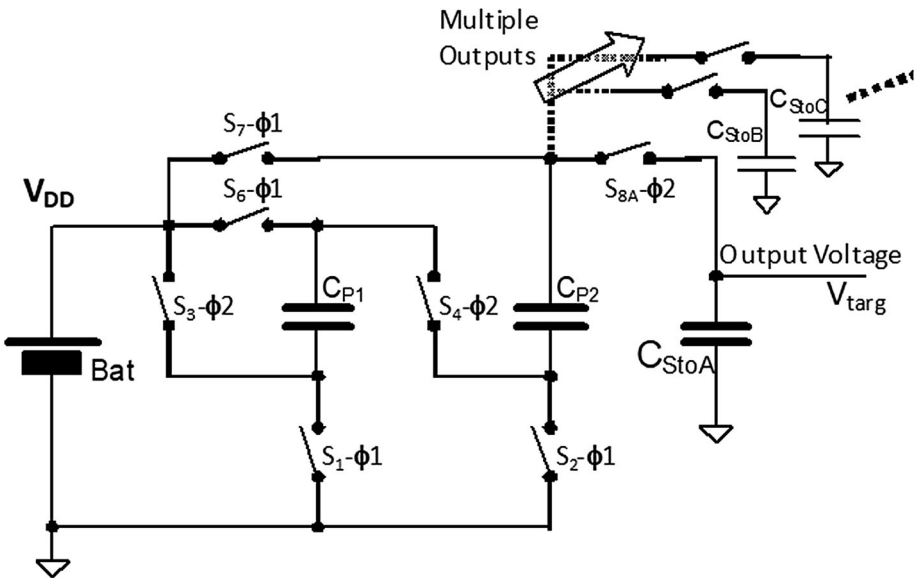


Fig. 13 Simplified scheme of a 3× charge pump with multiple output channels. ϕ1 (charge phase) and ϕ2 (pump phase) are non-overlapping phases

$$\eta_P = \frac{\langle P_{Load}\rangle}{\langle P_{Bat}\rangle} < \frac{V_{Targ}}{N.V_{DD}} = \eta_{Pmax}, \qquad \eta_Q = \frac{N\cdot\langle I_{Load}\rangle}{\langle I_{DD}\rangle} < 100\% \tag{5}$$

where N is the VM range (1 × , 2 × , 3 ×), P_{Load} and I_{Load} are the power and current consumption of a load in parallel with C_{Sto}. It follows that if $V_{DD} < V_{Targ} < 2{\bullet}V_{DD}$ then a voltage doubler increase the efficiency with respect to the 3 × or if $0 < V_{Targ} < V_{DD}$, the 1 × range results in a better efficiency as well. The VM in this work allows independent range and V_{Targ} configuration of each output. A complete block diagram of the circuit charging four storage output capacitors C_{StoX} (X = A, B, C, D) is shown in Fig. 14, while the detailed switch matrix section (a single output channel is shown for the sake of simplicity) is shown in Fig. 15. The VM is register-controlled with a SPI serial interface. Once a microcontroller (μC) starts the VM, a finite state machine (FSM) inside, generates with each clock period a control switch signals vector CS = {*SS1, SS2, SS5, SS7, SS8*} for the matrix in Fig. 15. The FSM supply voltage is V_{DD} thus the CS vector is in the {0, V_{DD}} domain. The FSM periodically cycles between states: Charge – Pump A – Charge – Pump B – Charge –…, and so on. Different switches configurations are selected to connect a single (1 × range), two series (2 × range), or two series + battery (3 × range) capacitors as depicted in Fig. 15 where the corresponding value of the switch signal

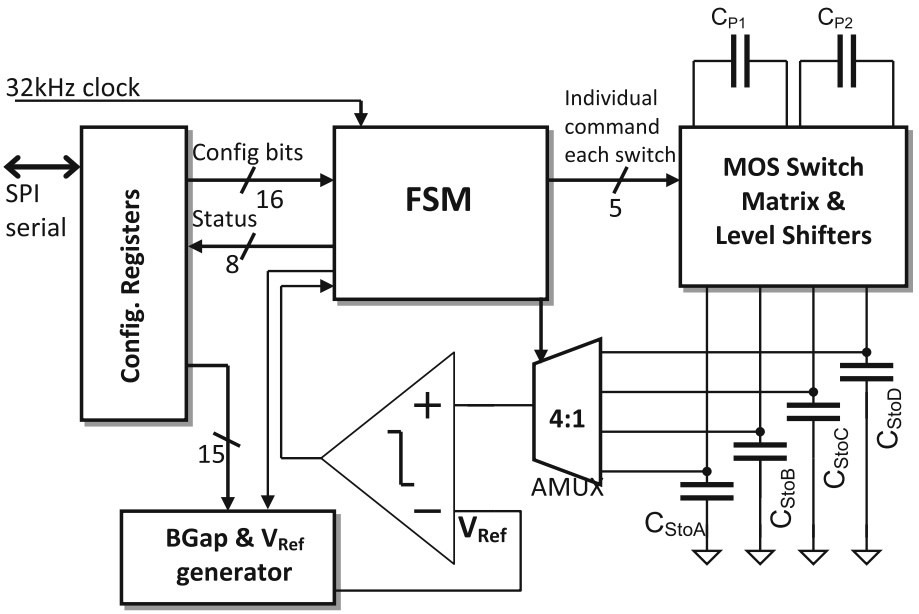
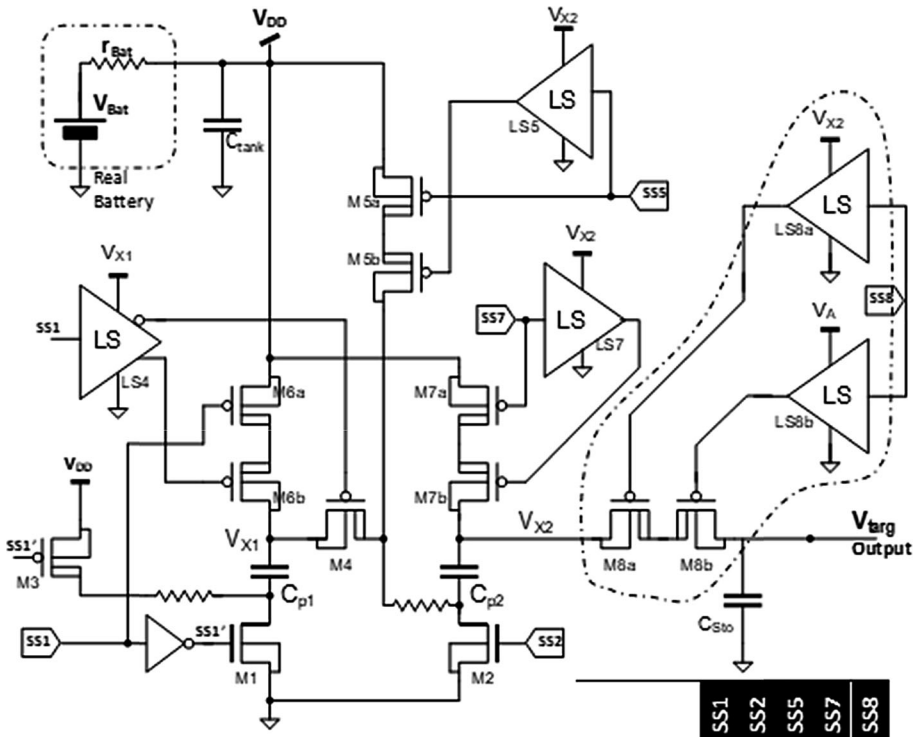


Fig. 14 Block diagram of the proposed Voltage Multiplier



	SS1	SS2	SS5	SS7	SS8
Charge	0	1	1	0	1
Pump 1X	0	1	1	1	0
Pump 2X	0	0	0	1	0
Pump 3X	1	0	1	1	0

Fig. 15 Detailed switching matrix section of the Voltage Multiplier. Only one channel output shown for the sake of simplicity

vector (CS) according to the programmed range is shown. V_{TargX} can be programmed in 32 voltage steps of the full-scale voltage that also is register-configured. A voltage comparator with a 5-bit programmable reference is used to determine charge-complete condition after each Pump state. On charge completion of all C_{StoX} the analog comparator is turned off and the clock of the FSM is halted for minimum steady state power consumption. The MOSFETS in Fig. 15 are each associated to a switch of Fig. 13 and FR-LS from Sect. 2 translating SSX low voltage signals to HV signal to command several gates (FR-LS are like that in Fig. 4 with the addition of a complimentary output when necessary). Composite (dual) switches are employed in several places to block the current flow in both directions at the off-state and small (120 Ω) resistors are connected in series to the current path to avoid undesired high current spikes that may introduce noise in analog circuitry. Transistor sizes were selected using simulated on-resistance

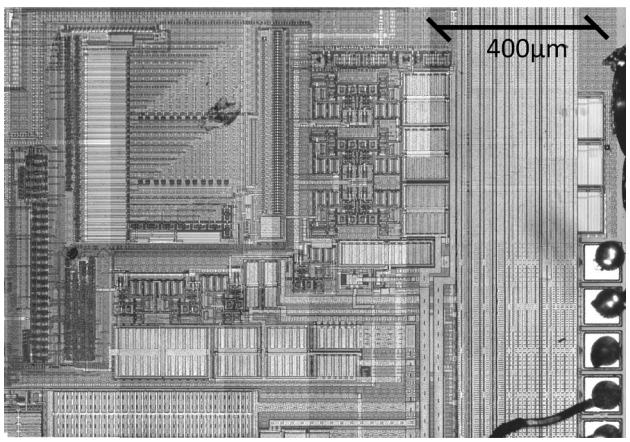


Fig. 16 Microphotography of the fabricated voltage multiplier

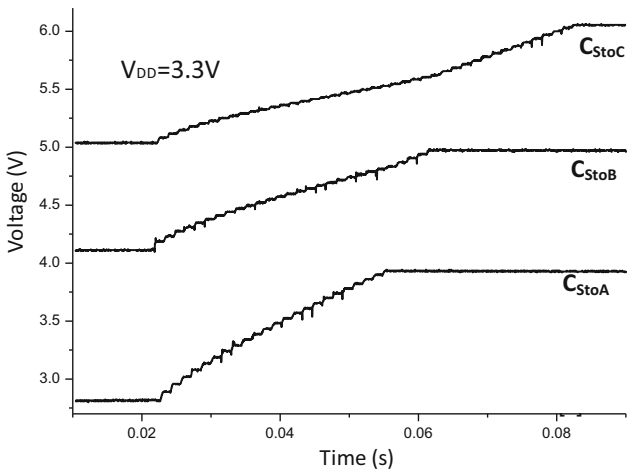


Fig. 17 Measured three channel capacitors charge transient of the VM for V_{DD} = 3.3 V

Table 4 Charge pump comparison between this work and previously published circuits [15, 15]

Characteristic	This work	[15]	[16]
V_{DD} (V)	$2 < V_{DD} < 5$	$2 < V_{DD} < 2.8$	$2.97 < V_{DD} < 3.3$
Output voltage (V)	0.1–16	0.25–4	3–12.6
Circuit area (pads not included)	1.7 mm^2	1.1 mm^2 (estimated)	2.87 mm^2
Active DC current consumption (μA)	0.6	2	n.a
Efficiency ($\eta_{P/}$ η_{Pmax})	85%	n.a	70%
Stages	1× ,2× ,3×	1× ,2×	1× ,2× ,3×

R_{ON} curves, the width was chosen to guarantee that total switch R_{ON} in the worst-case condition varying V_{DD} and transistor model (typical, worst-slow, worst-power (TM, WS, WP) foundry models). M_1, M_2 switches are medium voltage transistors sized W/L = 200 μm/1.4 μm, while the remaining are HV MOS transistors sized W/L = 500 μm/3 μm resulting in a worst-case $R_{ON} \approx 300\ \Omega$. The voltage detector in Fig. 14 compares each output capacitor voltage to a programmable reference V_{Ref} generated from a $V_{BGap} = 1.02 \pm 1\%$ bandgap reference [15], which is connected to a 32-tap resistor divider using 400 kΩ unitary poly resistors inside the V_{Ref} generator block of Fig. 14. A 32:1 analog multiplexer (AMUX) is utilized to select the adequate V_{Ref}. Since C_{StoX} can be charged up to 16.5 V, the output voltage is downscaled with a programmable 10MΩ grounded resistive divider inside AMUX to fit the bandgap range. The proposed circuit was fabricated and tested. Several V_{Bat}, range, and V_{targX} combinations were measured and the result closely fit simulations. Output voltages from 0.5 to 16 V, with V_{Bat} from 1.5 V to 5.5 V were tested. In Fig. 16 microphotograph of the VM is shown and in Fig. 17 the measurements of a simultaneous charge of 3 channels ($V_{targA} = 4$ V, $V_{targB} = 5$ V, and $V_{targC} = 6$ V) is shown, $C_{p1,2} = 220$nF, and $C_{StoX} = 10\mu$F in this experiment. Note that the output capacitor voltage resembles an exponential charge but after a capacitor completes its charge, the remaining capacitors charge faster because the FSM re-assigns the Pump time slots.

Several operating points were tested for different V_{DD}, V_{Targ}, range, load and capacitor values, with an average efficiency $\eta_Q = 97\%$, $\eta_P = 75\%$, and $\eta_P/\eta_{Pmax} = 89\%$ according to (5). In Table 4 the implemented programmable charge pump measurement result and characteristics are presented, including a comparison between this work and previously published VM [16, 17].

5 Conclusions

In this work the design, simulation, and measurement results, of three different level shifters (LS) covering a wide range of input and output operating voltages were presented. At a first glance the design of a LS seems simple, but a modified topology was developed, and a carefully transistor sizing was necessary to fully cover from 0 to 18 V output, and from 2 V to 5.5 V input. A full range level shifter (FR-LS) for an output V_H from 0 to 18 V, and a negative level shifter (NLS) for an output "low" V_{SS} down to (− 18 V) were developed. The circuits were fabricated in an isolated 0.6 μm HV-CMOS technology, and tested. Two application examples for implantable medical devices circuits were presented: a composite stimuli delivery switch for negative voltage pulse control, and a multi-channel integrated 5bit-programmable charge-pump voltage multiplier using external pump and storage capacitors. The charge pump takes advantage of the developed LS to efficiently command MOS switches, and shares the pump capacitors, achieving a measured efficiency above 95% in charge for all test points, and close to 90% of the maximum theoretical power efficiency. Target voltage, range, speed, can be programmed by an external CPU using a standard SPI interface to better adjust the circuit for a given medical device.

Acknowledgement The authors of this work would like to thank ANII FMV_2017_136543 for its funding, that made possible this research.

References

1. Maghsoudloo, E., Rezaei, M., Sawan, M., & Gosselin, B. (2017). A high-speed and ultra low-power subthreshold signal level shifter. *IEEE Transactions on Circuits and Systems I: Regular Papers, 64*(5), 1164–1172.
2. Matsuzuka, R., et al. (2017). An 80-mV-to-1.8-V conversion-range low-energy level shifter for extremely low-voltage VLSIs. *IEEE Transactions on Circuits and Systems I: Regular Papers, 64*(8), 2026–2035.
3. Lotfi, R., et al. (2018). Energy-efficient wide-range voltage level shifters reaching 4.2 fJ/transition. *IEEE Solid-State Circuits Letters, 1*(2), 34–37.
4. Thomas, S., Varghese, G. T. (2017). Design of optimum power, delay efficient level shifter for biomedical applications. In *2017 International Conference on Intelligent Computing, Instrumentation and Control Technologies (ICICICT)* (pp. 219–222). Kannur, India.
5. Novo, A., Gerosa, A., Neviani, A., Zanoni, E., Mozzi, A. (1999). Programmable voltage multipliers for pacemaker output pulse generation in CMOS 0.8 μm technology. In *25th European Solid-State Circuits Conference (ESSCIRC'99)* (pp.386–389). Duisburg, Germany.

6. Dommel, N., Lehmann, T., Wong, Y., Lovell, N., Byrnes-Preston, P., Suaning, G. (2006). Microelectronic retinal prosthesis: II. use of high-voltage CMOS in retinal neurostimulators. In *IEEE EMBS Conference* (pp.4651–4654). New York, USA.
7. Gak, J., Arnaud, A., Miguez, M., Mandolesi, P. (2017). Blind range level shifters from 0 to 18V. In *8th Latin American Symposium on Circuits & Systems (LASCAS)*. Bariloche, Argentina.
8. Luo, Z., & Ker, M. (2016). A high-voltage-tolerant and precise charge-balanced neuro-stimulator in low voltage CMOS process. *IEEE Transactions on Biomedical Engineering, 10*(6), 1087–1099.
9. Khorasani, M., et al. (2008). Low-power static and dynamic high-voltage CMOS level-shifter circuits. In *2008 IEEE International Symposium on Circuits and Systems* (pp. 1946-1949). Seattle, WA.
10. Kabirpour, S., & Jalali, M. (2020). A power-delay and area efficient voltage level shifter based on a reflected-output wilson current mirror level shifter. *IEEE Transactions on Circuits and Systems II: Express Briefs, 67*(2), 250–254.
11. Prutchi, D., Norris, M. (2005). Cardiac pacing and defibrillation *Design and development of medical electronic instrumentation*. Wiley.
12. CEN/CENELEC EN 45502–2 standard, *Active implantable medical devices – Part 2–1: Particular requirements for active implantable medical devices intended to treat bradyarrhythmia (cardiac pacemakers)"*
13. Merrill, D. R., Bikson, M., & Jefferys, J. G. (2005). Electrical stimulation of excitable tissue design of efficacious and safe protocols. *Journal of Neuroscience Methods, 141*(2), 171–198.
14. Wong, L. S. Y., Hossain, S., Ta, A. (2004). A very low-power CMOS mixed-signal IC for implantable pacemaker applications. *IEEE Journal of Solid-State Circuits, 32*(12), 2446–2457.
15. Miguez, M., Gak, J., Costa, G., Arnaud, A. (2012). A low-voltage, low-power 1.03V voltage reference for implantable medical devices. *Procs. EAMTA'12* (pp. 47–51). Cordoba, Argentina.
16. Novo, A., Gerosa, A., & Neviani, A. (2001). A sub-micron CMOS programmable charge pump for implantable pacemaker. *Analog Integrated Circuits and Signal Processing, 27*(3), 211–217.
17. Luo, Z., Yu, L., & Ker, M. (2019). An efficient, wide-output, high-voltage charge pump with a stage selection circuit realized in a low-voltage cmos process. *IEEE Transactions on Circuits and Systems I: Regular Papers, 66*(9), 3437–3444.

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