Integrated Programmable Current Source for Implantable Medical Devices

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***Abstract*— In this work, the design and implementation of a 25mA$_{(max)}$, 8 bits integrated programmable current source for implantable medical devices is presented. The proposed circuit includes a six-bits trimming mechanism to balance sink/source outputs to a precision below 1%. The current source is powered by an external supply voltage of up to 10V. The circuit was fabricated in a 0.18um HV CMOS technology, some preliminary measurements are also presented showing a close agreement with previously simulated results.**

Keywords—Current Source, Integrated Circuits, Implantable Medical Devices, Microelectronics.

I. Introduction

In recent years, there has been a remarkable growth in the research and development of new implantable medical devices (IMD) for the treatment of different pathologies [1]. Most active implants are battery powered embedded systems, which sense biological signals, and deliver stimuli to biological tissue. Stimuli are either current or voltage pulses (or pulse trains) to the patient ranging from a few hundreds of millivolts to well over 10 volts of voltage, or from a hundred microampere to tens of milliampere. Stimuli section of the circuit may consist of the basic elements shown in Fig. 1: a stimuli generator (either a voltage or current source), electrodes which connect the tissue to the device, a switch that toggles the electrical connection of the electrodes, and a control block that decides when and for how long a stimulus should be applied.

In this work, a *25mA* full-scale (positive-negative), 8-bits programmable integrated current source for implantable medical devices is presented including measurement results. The proposed circuit includes a 6-bits trimming mechanism to balance sink/source outputs to a precision below 1%. This circuit is part of an ASIC including also a micro-power RISC-V core designed to control modern IMDs implemented in a 0.18µm HV-CMOS technology. Current version of the ASIC includes a single output channel, but a modular design was chosen that can be easily extended to multiple channels. The current source can deliver source (positive to the electrode) and sink (negative from the electrode) current pulses or pulse trains, thus is composed of two almost independent current source blocks connected to tissue as depicted in Fig. 2. Initial specifications for the current source include a current absolute value error < 5%. While this value is relatively large, it is important to minimize the mismatch between the sink and source parts in Fig. 2 below 1% to reduce the net charge balance on the electrode to avoid tissue damage [2] (assuming a positive-then-negative current pulse each time). The net charge ideally should be zero but, in this case, a 1% error in a bipolar pulse is considered safe; however, the system may still require a later passive charge-balance stage [2] occasionally. Sink/source matching is a major restriction of the project; although both current sources are designed so that charge unbalance is null, variations in a real circuit may result in a significant error. Therefore, one of them is designed to be adjusted using the 6-bit trimming shown in Fig. 2. A trimming procedure is necessary to adjust these bits: first both sources in Fig. 2 are 8-bits programmed to the same value, then the lower source is trimmed to cancel the net charge in a positive-then-negative pulse. Depending on the IMD, a simple auxiliary circuit is necessary to measure the net charge during trimming. This procedure guarantees the required balance precision for a safe tissue stimulation. Initial specifications also include a $1\mu s$ or less settling time for the current source, and minimum crosstalk between multiple channels.

Each current source has 8 programming bits to select the desired current allowing 256 steps of $\approx 98\mu A$ each assuming a 25mA full-scale value. The programming bits are

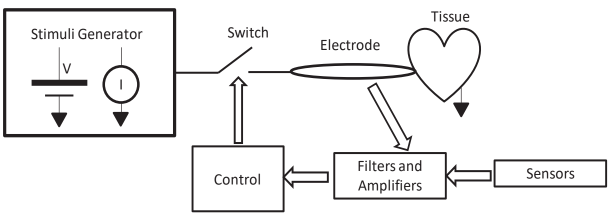

Fig. 1. Stimuli circuit basic blocks

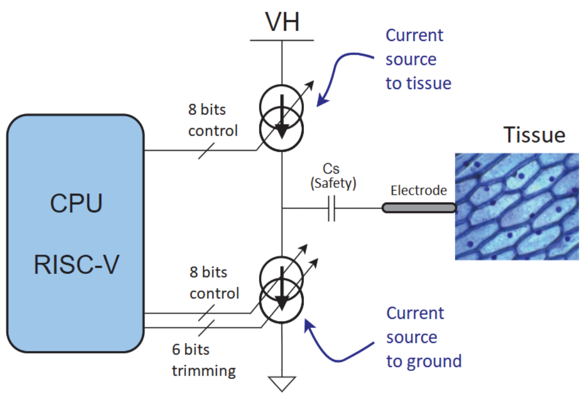

Fig. 2. Simplified circuit scheme.

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commanded by the CPU RISC-V core using 1.8V to 3.3V digital signals.

II. CURRENT SOURCE DESIGN

A. Sink source

Fig. 3 shows a programmable current source controlled by a digital to analog converter (DAC). A feedback loop sets the current through the load resistor R_{sens} by keeping the sensing voltage V_s equal to the reference voltage V_{ref} from the DAC, so the current I_d is [3]:

$$I_d = \frac{V_{ref}}{R_{sens}} \quad (1)$$

The main problem with this topology is the wide range of the voltage drop in the sensing resistor in a 256-steps programmable current, so in the proposed design, multiple branches are utilized as depicted in Fig. 4. The output current can be programmed by controlling the eight digital gates M_7 to M_0. This topology also eliminates the need of a DAC substantially reducing the total occupied die area and the power consumption. In Fig.4, for each branch the same fixed reference voltage is used thus the voltage drop is constant regardless the programmed current value. To achieve the desired output current, a voltage V_{ref} is set by the operational transconductance amplifier (OTA) [4], which controls the current thought the pass transistor ($M_{7\text{-}0}$). Each branch has half the resistance of the previous one to generate different currents. In the proposed circuit, the voltage V_{ref} = 200 mV, as low as possible to reduce power loss in the sense resistors, but high enough to reduce the impact of OTA's offset in the output current. A careful physical layout for the resistance was used to improve matching [5]. $M_{7\text{-}0}$ are medium voltage NMOS transistors (*nmma*), capable of withstanding voltage up to $V_{GS} = \pm\, 10V$, $V_{GD} = \pm\, 10V$, $V_{DS} = \pm\, 10V$.

The current that is delivered or taken from the tissue is the addition of each of the branches enabled. The minimum current is delivered if only b0 is enabled, while, to deliver the maximum current, all bits are enabled. The final current is:

$$I_{total} = \frac{V_{ref}}{R_{sens7}} \cdot b7 + \frac{V_{ref}}{R_{sens6}} \cdot b6 + \cdots + \frac{V_{ref}}{R_{sens0}} \cdot b0 \quad (2)$$

Knowing the resistance relation, we can rewrite (2) as:

$$I_{total} = \frac{V_{ref}}{R_{sens7}} \cdot b7 + \frac{V_{ref}}{R_{sens7} \cdot 2} \cdot b6 + \cdots + \frac{V_{ref}}{R_{sens7} \cdot 2^7} \cdot b0 \quad (3)$$

Where the gate b_i enables the i[th] branch, branch 7 being the one with the highest current and branch 0 with the lowest current. The current source to ground has 6 extra bits (trimming) for the fine tuning of the system by changing V_{ref}, and therefore the value of the current reducing the error between both sources to below 1%.

B. OTA design

The current through the sensing resistor is regulated by an *OTA* circuit (G_{mi} in Fig. 4) ant the transistor (M_i). This circuit uses a basic symmetrical *OTA*, like the one in [6] and the ACM model [7] was used for transistor sizing. The OTA is intended to have a fast response ($< 1\mu s$), low power consumption ($< 100\mu A$) and offset below 1% of the reference voltage V_{ref} ($< 2mV$). The *OTA* supply voltage may vary between 2.8V and 3.3V (typical values for IMDs batteries), and all 8 OTA have the same layout but with different bias currents, thus reducing design time while not having a meaningful impact on the overall area of the system.

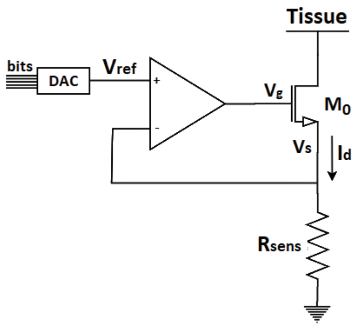

Fig 3. Schematic circuit of a classic current source.

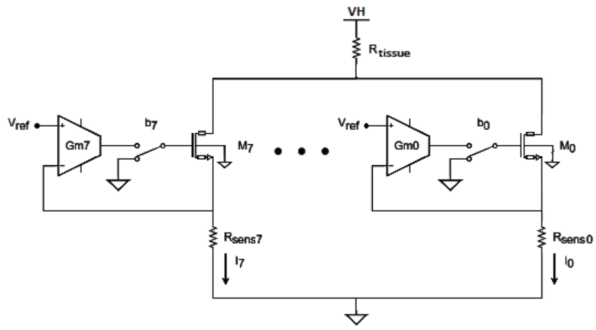

Fig. 4. Simplified schematic of the implemented current source.

C. Trimming

To generate the voltage V_{ref} a current I_{ref} is injected through a reference resistor (R_{ref}). R_{ref} is implemented as several trimming resistors (R_{trim}) connected in series. These resistors are matched with the sensing resistors (R_{sensi} of Fig. 4) to reduce variations. The fine-tuning is implemented by 6 bits that can change the value of the reference resistance and thus vary V_{ref}, as shown in Fig. 5. These allows 64 steps of ~1,5mV to adjust the reference voltage to maintain a current source balance error of less than 1%. The minimum voltage and maximum V_{ref} values are 150mV and 247.6mV respectively. The final value of V_{ref} is selected to determine the absolute value of the current (bellow 5% error).

D. Source source (high voltage)

The current source is connected directly to a high voltage V_H = 10V, as shown in Fig. 2, while the rest of the power supplies are similar to the sink source, it has a reference current I_{ref} = 50nA [8] and a voltage V_{dd} = 3.3V for the control logic. The design used for this source is analogous

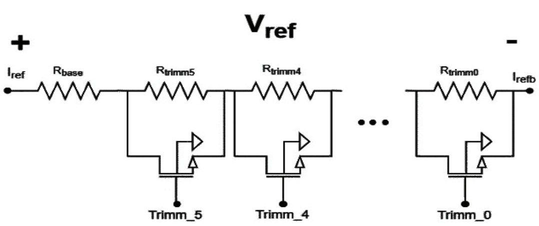

Fig. 5. Fine tuning system's schematic

(symmetric) to the sink source, a single branch is shown in Fig.6 for the sake of for simplicity.

The design of the OTAs for the high voltage source is also similar to the sink source's OTAs, but in this case, a medium voltage NMOS differential pair was selected, to withstand the high voltage.

Due to the use of high voltage signals, Level Shifters (LS) following the guidelines in [9] were designed for the control logic. LS1 and LS2 in Fig. 6 have complementary inputs. When LS1 is activated, M_7 gate is connected to the output of the OTA closing the control loop delivering the stimuli. When LS2 is activated, M_7 gate is connected to VH, opening the M_7 transistor thus reducing the output current to 0. To avoid shorts, LS1 and LS2 go into high impedance mode when the other is activated.

III. Simulations and Measurement Results

The on/off delay times for different stimulation currents are shown in Table I. In Fig 7, minimum, maximum and mid value of possible current stimuli are shown for sink and source cases. All the simulations were performed at a 37°C temperature and all results are within design specifications, except for a slightly larger settling time in some cases, but less than $2\mu s$. The current spikes are too short to cause damage to the tissue.

TABLE I. On and off times for different output currents

Currents	Source		Sink	
	ON (µs)	*OFF (µs)*	*ON (µs)*	*OFF (µs)*
25 mA	1.10	0.40	0.99	0.31
12.5 mA	1.04	0.20	0.80	0.18
98 µA	0.50	0.10	1.90	0.10

The final circuit layout is shown in Fig. 8. The sink current source (red box) occupies a total area of $0.276mm^2$ and the source current source (yellow box) occupies a total area of 0.839 mm^2. The complete circuit area is 1520µm x 1520µm, including PADs, ESD protection cells and other circuits for a different project. The circuit was fabricated in a 0.18µm CMOS technology and tested. The chip shown in Fig. 8 is only includes the analog components of the stimulator, a different die was used for the RISC-V CPU for testing purposes. Initial measurement results are shown in Table II for three different stimuli current values: maximum (25mA), minimum (98µA) and an arbitrary intermedium (12.5mA, denoted Mid) current for both sources. In the table, "T" is the target current and "M" is the measured current. A simple resistor was utilized as the tissue model for simulation. The settling times are presented in Table III. The times shown are an average of 5 different measurements under the same conditions. Multiple pulses measured are shown on Fig. 9.

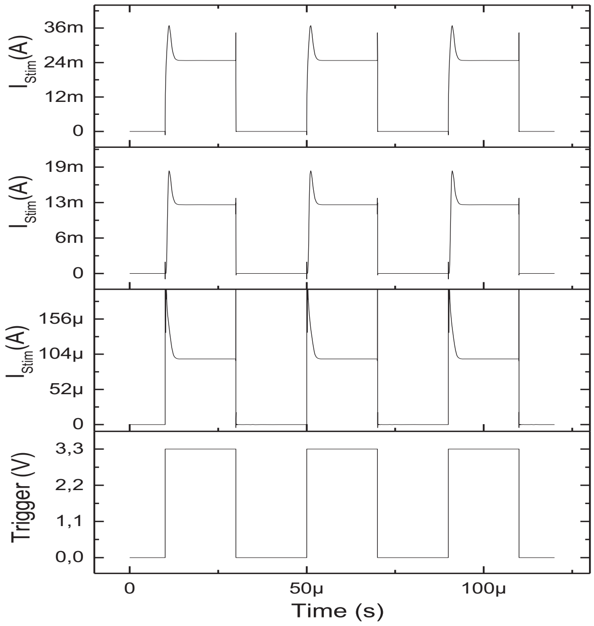

Fig. 7. Simulation of min, mid and max currents for the source to tissue source.

TABLE II Max. med and min currents for both sources

Current Source	Max current (mA)		Mid current (mA)		Min current (µA)	
	T	*M*	*T*	*M*	*T*	*M*
Sink	25	25	12.5	13	98	107
Source	25	25.3	12.5	13.2	98	120

TABLE III. Response time of both sources

Current Source	Response time (µs)		
	Max current	*Mid current*	*Min current*
Sink	1.273	0.860	1.551
Source	1.380	2.548	0.680

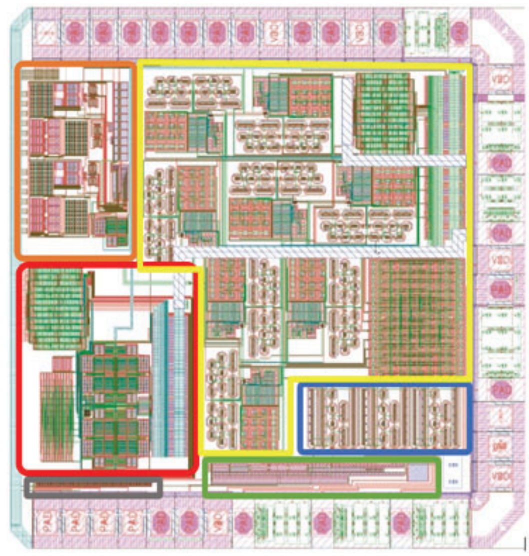

Fig. 8. Layout of the complete chip. Red: Current source to ground, Yellow: Current source to tissue, Blue: Level shifters, Green: Iref source, Gray: Registers and Orange: Linearized amplifier.

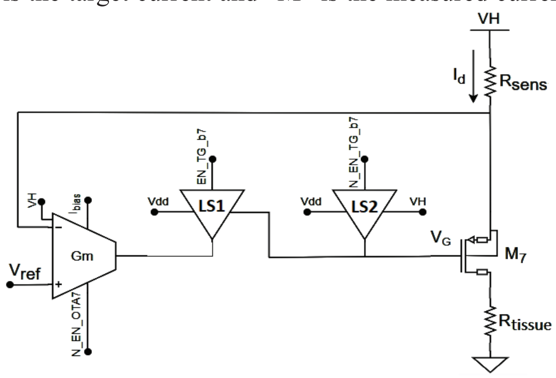

Fig. 6. Branch number 7 of the current to tissue source

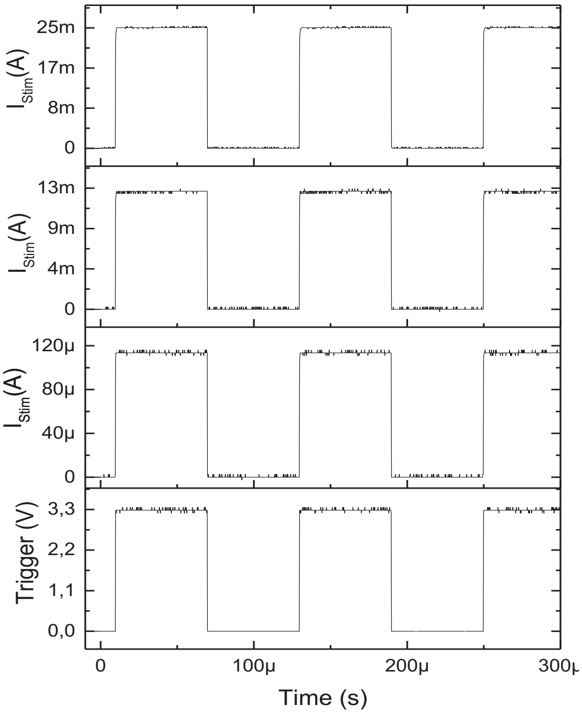

Fig. 9. Measured minimum, mid, and maximum current pulses for the source to tissue source.

Finally, the crosstalk currents between sources were measured. The crosstalk is defined as the charge (current) injected to an electrode trough an ideally open circuit, when another channel stimulates the same tissue with another electrode. To measure crosstalk, one of the sources is turned on and the current in another source is measured. In Fig. 10 a measured crosstalk current plot from the source current source is presented. The crosstalk current shown was generated when the sink current source was turned on for 100 µs at 25 mA, while the measured source was turned off. Table IV displays the total charge delivered from the turned off source by the crosstalk current (ideally this should be as low as possible). Multiple crosstalk cases were measured with different currents delivered from the turned-on source. In Table IV the cases when the turned-on source delivers its maximum and mid currents is presented, as at minimum current, crosstalk was negligible.

TABLE IV. TOTAL CHARGE DELIVERED FROM CROSS TALK CURRENTS

Total charge (nC)			
Turned on source		*Crosstalk source*	
	Current	*Source*	*Sink (3.3V)*
Source	Max	-	0.359
	Mid	-	0.154
Sink (3.3V)	Max	0.201	-
	Mid	0.177	-
Sink (2.8V)	Max	0.293	-
	Mid	0.189	-

IV. CONCLUSIONS

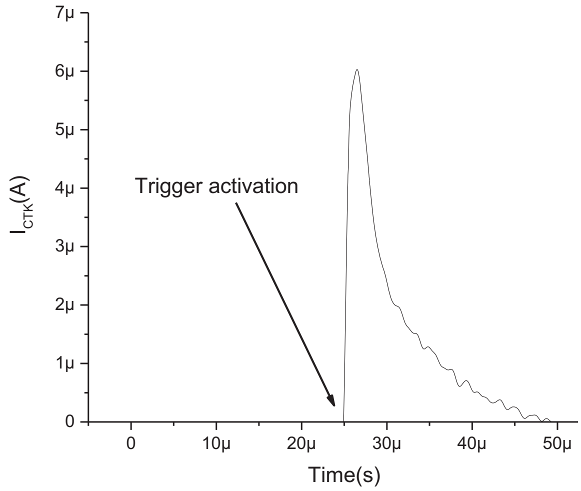

Fig. 10. Crosstalk current from source to ground source when the source to tissue source is on at 25 mA fot 100 µs.

This paper presents the study, design, simulations and measurements on a fabricated circuit, of a programmable current source for implantable medical devices in a 0.18µm CMOS HV technology. The current source can deliver a current between $98\mu A$ and $25mA$ in steps of $98\mu A$ (8 bits). fine-tuning system of the current source to ground is controlled with another 6 bits to minimize the error to less than 1% with respect to the other source. The worst case ($25mA$ stimuli) the measured settling time is $1\mu s$ to ± 10% except for the branch 0 of the source to tissue, which is slightly larger.

The complete chip was fabricated in a total area of $2.31mm^2$ including PADs and ESD protection.

REFERENCES

[1] Freedonia Group, Implantable Medical Devices, Study number: 2852 Cleveland Ohio, 2015.

[2] D. R. Merrill, M. Bikson y J. G. Jefferys, “Electrical stimulation of excitable tissue: design of efficacious and safe protocols,” Neuroscience Methods, pp. 171-198, 2005.

[3] J. Osta, J. Suarez, M. Miguez and A. Arnaud, "Integrated programmable current source for implantable medical devices," 2009 Argentine School of Micro-Nanoelectronics, Technology and Applications, San Carlos de Bariloche, pp. 56-60, 2009.

[4] B. Razavi, “Integrated Circuits, Design of Analog CMOS,” p. 146, 2017.

[5] A. Hastings, “The Art of Analog Layout” 2nd, Pearson, 2005.

[6] J. Gak, M. Miguez, A. Arnaud, “Nanopower OTAs With Improved Linearity and Low Input Offset Using Bulk Degeneration,” Circuits and Systems I: Regular Papers, IEEE Transactions on, 1-10, 2014

[7] C. Galup-Montoro y M. C. Schneider, “Mosfet modeling for circuit analysis and design,” World Scientific, pp. 370-373, 2007.

[8] E. M. Camacho-Galeano, C. Galup-Montoro and M. C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 2, pp. 61-65, Feb. 2005.

[9] J. Gak, M. Miguez, A.Arnaud y P. Mandolesi, “Blind range level shifters from 0 to 18V,” Latin American Symposium on Circuits and Systems, Bariloche, Argentina, Feb. 2017