The RISC-V in implantable medical devices

Abstract — **In this work, first, the case of implantable medical devices (IMDs) will be presented including state of the art and industry overview. The main characteristics of IMD ASICs are discussed (technical, engineering, business point of view). Then a RISC-V 32RVI based microcontroller, targeting medical devices, is presented, designed in a 0.18µm HV-CMOS process combined with several biological tissue stimuli and sensing circuits. The microcontroller, which includes SPI, UART and GPIO interfaces, a packet-based bus and memory controller, and 8kB SRAM, was optimized for area, and power consumption. The complete test chip (analog+RISC-V) occupies a 5mm^2 area but only 0.82mm^2 correspond to the RISC-V controller, which operates up to 20MHz, with average energy needs of less than 34 pJ/cycle (3pJ STD), and for which several reliability and safety issues were considered. As far as we know this is the first RISC-V based designed aimed at medical applications proposed.**

Keywords— implantable medical devices, CMOS HV, RISC-V, current source, biomedical circuits.

I. Introduction

A block diagram of a generic implantable medical device (IMD) is shown in Fig. 1, which includes electrodes connecting the tissue to the device through one or multiple pass-switches, sensors, amplifiers and filters for the signal conditioning of body's natural electrical activity, an intelligent control logic (CPU) deciding when and for how long a stimulus should be applied, a nowadays complex telemetry block communicating data with the doctor when necessary, and a stimuli section composed of voltage and/or current sources. In the case of mature products like pacemakers or cochlear implants and large IMD manufacturers, both the microcontroller and sensing/stimuli circuits are integrated in the same SoC. If not the case, an off-the-shelf microcontroller is utilized either combined or not with an analog ASIC for sensing/stimuli functions [1], but the option unnecessarily increases power consumption, PCB size, and production cost. The main characteristics of an IMD ASIC are:

- Usually implemented in a HV technology capable to handle up to 20V as necessary for tissue stimulation.
- Micropower consumption because the battery should last for years.
- Safety and reliable circuits and systems. A reliable circuit is less likely to fail; a safety compliant circuit means it will not result harmful for the patient even in the case of a single failure even occurs.
- Very low volume production (thousands to hundreds of thousands) to share the cost of the ASIC development.

In this context, an open source, scalable processor like RISC-V would be helpful to allow small to large companies to develop their own ASICs. While a 32 bits CPU may sound complex or power hungry, recent advances in Application Specific Processors (ASP) allow to implement efficient controllers even for the case of medical applications. The idea is to remove unnecessary features like floating point capabilities, predictive execution modes, superscalar pipelines, multi-level cache and/or DMA, etc. As pointed by [2], this kind of design strategy enhances system reliability and makes simpler to make the system safe. In Fig.2 the designed SoC topology is shown. The target technology is a 0.18µm HV-CMOS process including FLASH memory capabilities as necessary for commercial applications. The circuit includes a custom RISC-V core, 8kByte SRAM (no FLASH at this stage), a HV sink and source 8-bit programmable + 6 bits trimmable current source (8 channels), and a 4bit HV port using level shifters (LS) capable to translate from the 1.8V

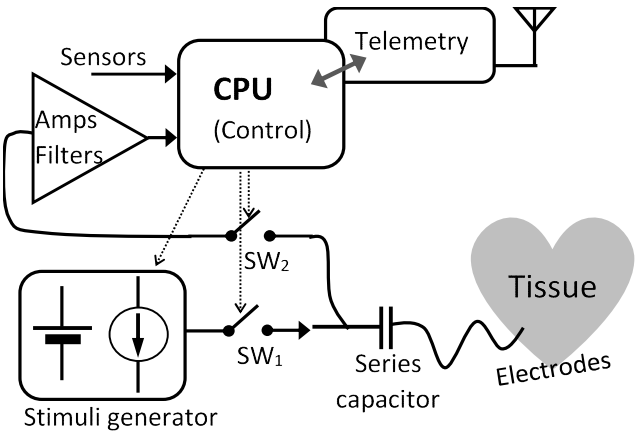

Fig. 1. Simplified block diagram of an IMD.

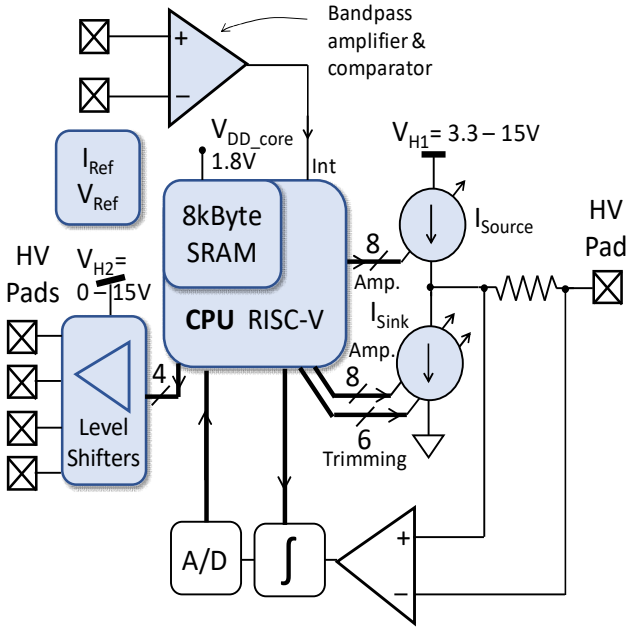

Fig. 2. The designed IMD SoC topology (colored blocks being fabricated).

core supply to a wide range V_{H2} from 0 to 15V. A programmable ULP bandpass amplifier and comparator block were also included, as well as a programmable current sensing amplifier, and AD converter. The RISC-V core, a single channel current source, 4 bits LS, bandpass amplifier and comparator, are being fabricated in the current version of the chip occupying a 5mm^2 (0.82mm^2 RISC-V core).

II. The Developed RISC-V RV32I based Microcontroller

Siwa, a custom 32-bit microcontroller unit based on an in-house, from scratch, RTL implementation of the RISC-V RV32I open architecture was used as the central control unit for the IMD previously described. The processing unit presented at the block level in Fig. 3, includes a main control unit (MCU), 8 kB SRAM, a memory and bus and controller unit (MBC), an ALU intended for integer arithmetic, a timer, and an interruption handler. The CPU interfaces the memory mapped I/O units through a central bus; every communication coming from the system to the CPU is stored in a queue that may be accessed through custom CSRs and trigger an interruption. The CPU is single threaded, with 53 instructions and a control and status register (CSR) from the standard RISC-V ISA. The standard I/O interfaces included in the system are a UART, an SPI and 8 GPIOs; also, dedicated input/output channels controllable using custom CSRs are included for the high-voltage tissue stimulators. Interrupts can come from external devices connected to the bus (SPI or UART), from the internal timer, and from an external pin. The bootstrap process for the system is carried on through an external serial flash memory connected to the SPI interface. The microcontroller preliminary RTL design was fully tested on a FPGA (including bootstrap and I/O, running several compiled applications), and then verified using a UVM framework. The chip is implemented using 1.8V low power library cells: there are four separate voltage domains to allow for independent power control, including the SRAM's, and providing 3.3V digital interfacing to the analog stimulus circuits. The total cell count is 11817, excluding pads and the SRAM. The estimated average energy consumption per clock cycle is under 34pJ/cycle, well under what is typical for common complete microcontrollers in the IMD industry, such as the MSP430, at 803pJ/cycle, as reported in [3].

III. Conclusions

RISC-V may result an attractive option for the development of fully integrated IMD-SoCs because of engineering cost and its flexibility. At the present, the complexity of IMDs is increasing to such an extent that the development cost/effort of an ASIC cannot be easily addressed using commercial IPs or custom processors, because this cost/effort is shared between a reduced number of fabricated chips. Also, reliability and safety issues require the capacity to customize the target processor. In this work, a RISC-V core processor combined with biological tissue stimuli and sensing circuits in a 0.18µm HV CMOS technology were presented. The objective was to validate a flexible platform for the development of highly integrated IMDs, combining available RISC-V open resources and custom analog circuit blocks in a SoC.

Acknowledgment

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References

[1] D.Prutchi y M.Norris, "Cardiac Pacing and Defibrillation" in *Design and Development of Medical Electronic Instrumentation*, Wiley-Interscience, 2005, ISBN: 9780471676232.

[2] C. Strydis, R.M. Seepers, P. Peris-Lopez, D. Siskos, I. Sourdis, "A system architecture, processor, and communication protocol for secure implants," ACM Transactions Architec. Code Optim., vol.10, no.4, pp.1-23, Dec. 2013.

[3] C. S. Mestais, G. Charvet, F. Sauter-Starace, M. Foerster, D. Ratel, and A. L. Benabid, "WIMAGINE: Wireless 64-channel ECoG recording implant for long term clinical applications," IEEE Transactions on Neural Systems and Rehabilitation Engineering, vol. 23, no. 1, pp. 10–21, Jan 2015.

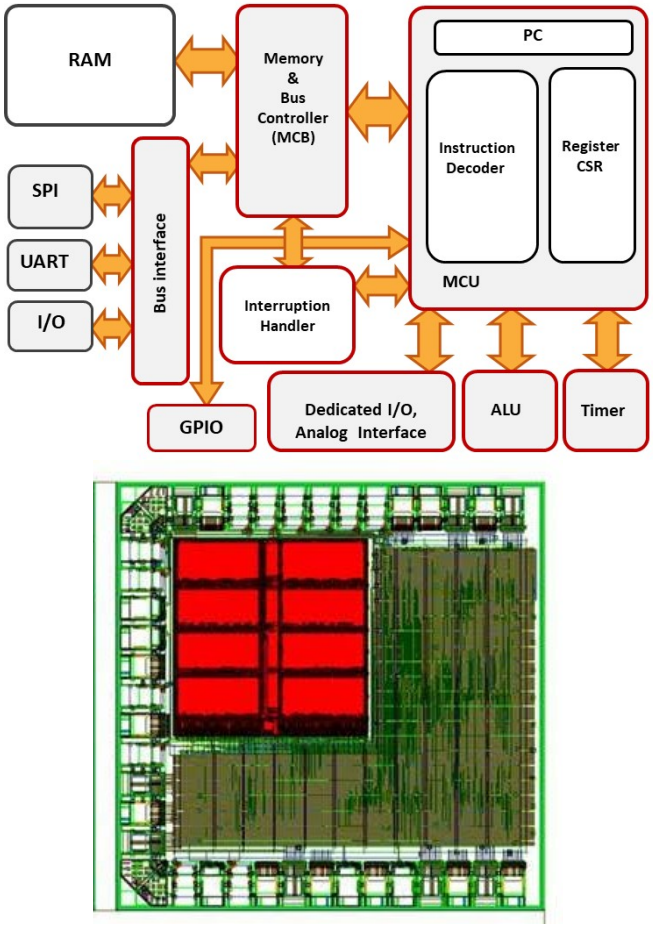

Fig. 3. Block diagram of Siwa, the RISC-V RV32I based microcontroller designed as the IMD controller, and 2.2×2.2mm^2 (core+SRAM+PADs) layout image.