Module for Stimuli Control of an Integrated Programmable Current Source for Implantable Medical Devices

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Abstract

Implantable Medical Devices (IMDs) have been widely deployed in both novel and established applications. Ranging from cardiac defibrillators, pacemakers and cochlear implants to gastric and neurostimulators, these devices are being improved through the developments in microelectronics, biotechnology, medicine and materials.

In this work, two multipurpose integrated current generators for IMDs designed by the Microelectronics Group at the Universidad Católica del Uruguay are fully characterized and validated. These current sources are capable of extracting and delivering a wide range of outputs from hundreds of µA to tens of mA making them suitable for different clinical applications. The measured parameters include the output current range and precision, supply voltage range, output voltage range, bias current dependence, response times, current consumption and crosstalk.

The second part of this project consists of the design of a calibration module to be appended to the current sources. The purpose of this module is to detect any current mismatch between the sourcing and sinking stimulation phases which can lead to tissue damage over time. Once measured, the current difference can be reduced by means of the trimming mechanism integrated in the current sources' design. The calibration module was implemented as a Switched-Capacitor (SC) amplifier and was submitted for manufacturing in XFAB's XT018 180 nm CMOS technology. The circuit can also be easily adapted to function as an Electrode-Tissue Interface (ETI) impedance measurement device.

Keywords **-** Current Source, Current Calibration, Integrated Circuits, Implantable Medical Devices, Microelectronics, XFAB

Resumen

Los Dispositivos Médicos Implantables (IMDs, por su sigla en inglés) han tenido un amplio desarrollo en sus aplicaciones originales y en nuevas áreas. Desde desfibriladores cardíacos, marcapasos e implantes cocleares hasta neuroestimuladores y estimuladores gástricos, estos dispositivos están siendo mejorados a través de los avances en microelectrónica, biotecnología, medicina y materiales.

En este trabajo se realiza la caracterización completa y validación de dos generadores de corriente integrados multipropósito para IMDs diseñados por el Grupo de Microelectrónica de la Universidad Católica del Uruguay. Las fuentes son capaces de extraer y entregar un amplio rango de corrientes desde cientos de µA hasta decenas de mA, lo que las hace adecuadas para diferentes aplicaciones médicas. Se midieron parámetros tales como el rango y precisión en la corriente de salida, rango de tensión de alimentación, rango de tensión de salida, dependencia con la corriente de polarización, tiempos de respuesta, consumo de corriente y diafonía.

La segunda parte de este proyecto consiste en el diseño de un módulo de calibración para incorporar a las fuentes de corriente. El propósito de este módulo es detectar diferencias entre la corriente inyectada y extraída que con el tiempo pueda conducir a daños en el tejido biológico. Una vez medida, es posible actuar para reducirla mediante el mecanismo de ajuste fino integrado en el diseño de las fuentes de corriente. El módulo de calibración se implementó como un amplificador con Capacitores Conmutados (SC, por su sigla en inglés) y se envió a fabricar en la tecnología CMOS XT018 de 180 nm de XFAB. El circuito puede ser adaptado fácilmente para funcionar como un dispositivo de medición de impedancia de la interfaz electrodo-tejido (ETI, por su sigla en inglés).

Palabras Clave - Fuente de Corriente, Calibración de Corriente, Circuitos Integrados, Dispositivos Médicos Implantables, Microelectrónica, XFAB

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Index

1 Introduction **11**
- 1.1 Implantable Medical Devices . . . 12
- 1.2 Tissue Stimulation . . . 12
  - 1.2.1 Charge Balance and Current Stimulators . . . 12
- 1.3 Electrical Model of the Electrode-Tissue Interface . . . 13
  - 1.3.1 Resistor Model . . . 13
  - 1.3.2 Resistor–Capacitor Model . . . 13
- 1.4 Objective and Framework . . . 14

2 Characterization of the Integrated Programmable Current Sources **16**
- 2.1 Introduction . . . 17
  - 2.1.1 Current Sources . . . 17
    - 2.1.1.1 Requirements . . . 17
    - 2.1.1.2 Design Characteristics . . . 18
- 2.2 Measurements . . . 20
  - 2.2.1 Setup . . . 20
    - 2.2.1.1 First Version . . . 20
    - 2.2.1.2 Second Version . . . 22
  - 2.2.2 Results . . . 24
    - 2.2.2.1 Bias Current - Output Current Relation . . . 24
    - 2.2.2.2 Output Current Range . . . 26
    - 2.2.2.3 Trimming Mechanism . . . 28
    - 2.2.2.4 Supply Voltage Range . . . 29
    - 2.2.2.5 Current Consumption . . . 31
    - 2.2.2.6 Response Times . . . 33
    - 2.2.2.7 Output Voltage Range . . . 34
    - 2.2.2.8 Crosstalk . . . 35
  - 2.2.3 Simulated Trimming Model for Current Adjustment . . . 35
- 2.3 Conclusions . . . 37

3 Design of the Calibration Module **38**
- 3.1 Introduction and Initial Requirements . . . 39
- 3.2 Output Voltage Measurement . . . 41
- 3.3 Operation Requirements . . . 44

3.4 Considered Designs . . . 45
3.5 Computation of the Gain . . . 49
3.6 Global Operation . . . 50
3.6.1 Simulation of the Ideal Circuit . . . 50
3.6.2 Capacitor Selection . . . 51
3.6.3 Design of the Switches . . . 52
3.6.4 Correlated Double Sampling . . . 54
3.6.5 Digital Design . . . 56
3.6.6 Design of the Operational Amplifier . . . 59
3.6.7 Final Design . . . 63
3.7 Conclusions . . . 65

4 Layout of the Calibration Module 66
4.1 Capacitors . . . 67
4.2 Operational Amplifier . . . 68
4.3 Switches . . . 69
4.4 Digital Block . . . 70
4.5 Pads and Buffers . . . 70
4.6 Complete Chip . . . 73

5 Setup for the Characterization of the Calibration Module 75
5.1 Measurement and Operation Setup . . . 76
5.2 Measurement Plan . . . 78

6 Conclusions 80
6.1 Characterization of the Integrated Programmable Current Sources . 81
6.2 Design of the Calibration Module . . . 81
6.3 Future Work . . . 83
6.3.1 Improvements to the Calibration Module . . . 83
6.3.2 Redesign for High Voltage . . . 83
6.3.3 Module for Impedance Measurement . . . 83

7 Acronyms 85

8 References 88

9 Annex 92
9.1 Roadmap . . . 93
9.2 Firmware for the Microcontroller . . . 93
9.3 PCB for the Second Version of the Current Source . . . 101

9.4 Design of the Current Sources' Trimming Mechanism 102
9.4.1 First version 103
9.4.2 Second version 104

Part 1

Introduction

1.1 Implantable Medical Devices

Since the development of the first artificial cardiac pacemaker in the 1950s, there have been significant advances in the understanding and manufacturing of Implantable Medical Devices (IMDs) and in the medical treatments based on their use [1]. Besides cardiac pacemakers, cardio defibrillators, cochlear implants and neurostimulators are also some examples of the IMDs that are being currently developed and implanted [2] [3] [4].

Active IMDs are defined as electronic medical devices that are capable of being introduced, surgically or medically, into the human body [2]. Since they are intended to remain inside the body after the procedure, IMDs must be reliable, safe, compact in size and reach low levels of power consumption. These limitations make microelectronics a fundamental tool for the development of new technologies in the field.

1.2 Tissue Stimulation

Most IMDs work by stimulating the biological tissue with voltage or current pulses transferred by electrodes [5]. It is possible to implement a feedback loop to control these stimuli based on measurements taken from sensors [6]. A Central Processing Unit (CPU) is generally integrated in the IMD to program the triggering of the stimuli and implement other functionalities such as control, telemetry and energy management. Figure 1 shows a typical stimulation system for an IMD.

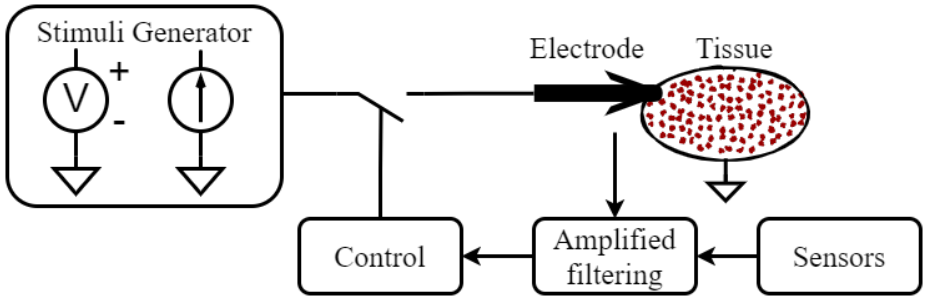

Figure 1: Typical stimulation diagram for an IMD (from Reference [6]).

1.2.1 Charge Balance and Current Stimulators

Both current and voltage stimulation produce electrochemical effects on the tissue. To reduce the risk of possible damages, the net charge transferred to the tissue by the end of the stimulation process should be minimal [7].

Current stimulation allows a direct control of the charge transferred to the tissue. Voltage stimulators, in turn, exchange a net charge that is dependent on both tissue and electrode impedance. Therefore, for many applications current stimulators are preferred over voltage stimulators [7].

In order to achieve a charge-balanced stimulation, some IMDs rely on biphasic pulses. The working principle is based on passing a current in one direction and then reversing it in the following phase. It has been shown that this specific type of stimulation does not cause detectable tissue damage at levels up to $2\frac{\mu C}{mm^2}$ per pulse [7].

Assuming that both phases are symmetrical in terms of duration, the charge delivered to the tissue during the first phase of the pulse will ideally match the charge extracted during the opposite phase provided that both current amplitudes are equal. In practice, a 1% error in a biphasic pulse is generally considered safe [6].

The fundamental parameters defined for current stimulation are the intensity, duration, duty cycle and frequency of the pulses generated. The values of these parameters may vary according to the pathology being treated. The current generally ranges from a few hundred µA to tens of mA and the pulse duration can be as low as a few µs and up to tens of ms [8].

1.3 Electrical Model of the Electrode-Tissue Interface

The Electrode-Tissue Interface (ETI) is a complex environment that consists of the electrode, its adhered tissue cells and biochemical reactions [9]. This has been the subject of much study and further developments are expected.

An electrical characterization of the ETI is necessary not only to model the behavior of the electrode-tissue impedance while undergoing stimulation, but also to monitor possible malfunctions. This impedance is affected by multiple factors such as the material and shape of the lead tip, the type of tissue being stimulated and the value and frequency of the current used for the stimulation [10]. Over time, it may also be affected by other factors such as tissue edema. Abrupt changes in the value of this impedance, however, can be indicative of lead malfunction [1].

1.3.1 Resistor Model

A simple and accurate way to model the ETI impedance is by a single resistance [10] whose value can range anywhere from $200\,\Omega$ up to $5\,k\Omega$ [11] [12]. This resistor accounts for all of the effects involved in the distribution of charge and leakages at the interface.

Other more complex electrical models for the ETI are proposed in the literature [13]. In particular, for sinusoidal inputs, the ETI may be represented with resistive and reactive components [10] [14] [15] [16] [17] [18].

1.3.2 Resistor–Capacitor Model

The Resistor-Capacitor (RC) model is shown in Figure 2. In this circuit, C_d represents a double-layer distribution of ionic charge at the ETI. R_d models the leakage

across the double layer and R_s models other resistance effects at the interface [10]. Usually C_d ranges from a few nF to a few hundred nF, R_d is generally a few tens of kΩ and R_s ranges from a few hundred Ω to a few kΩ [10] [19].

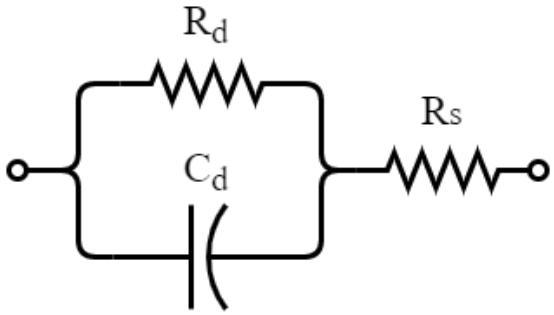

Figure 2: RC circuit modelling the ETI impedance.

Unlike the resistor model, the circuit from Figure 2 represents the ETI as frequency-dependent. At high frequencies, however, the equivalent impedance can be approximated to R_s. At low frequencies, the equivalent impedance is larger, roughly $R_s + R_d$.

Using this approximation and for simplicity the resistor model is selected in this work to simulate the ETI.

1.4 Objective and Framework

Based on the stimulation schemes referred to in the previous sections, an additional module is designed in this work to improve an existing current stimulator. It acts as an automatic calibration system that minimizes the net charge transferred to the tissue to acceptable ranges.

The current stimulator where the module will be integrated is implemented following the simplified stimulation diagram of Figure 3. It is designed as two programmable current sources capable of generating a biphasic pulse. One current source delivers current to the tissue while the second source extracts the injected current from the tissue. These stimulation phases will be referred to as "sourcing" and "sinking", respectively.

The safety capacitor of Figure 3 ensures that in case any of the current sources fail, no direct current is delivered to the tissue [20]. This capacitance is required to be on the order of a few µF. In this design a 1 µF capacitor is used for the simulations. The implementation of this security measure does not belong to the scope of the design.

Additionally, the current sources described are implemented along with a CPU with a Reduced Instruction Set Computing (RISC) architecture. Its main function is to program the output values for the current sources. Having the option to

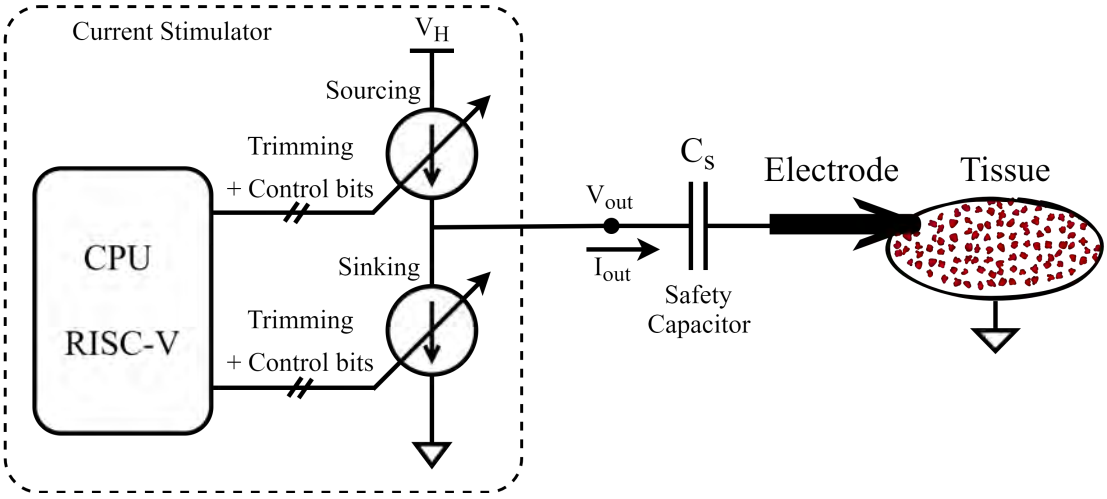

Figure 3: Simplified diagram for the integrated programmable current stimulator (from Reference [6]).

program different current outputs implies that the same device can not only be adapted to the needs of each patient, but it can also be used to treat different pathologies and to stimulate different types of tissues.

The two internal current sources are designed so that both phases in the stimulation can be matched ideally to avoid delivering a net direct current to the tissue. In practice, however, variations due to non-idealities can arise and thereby break this balance. Therefore, in order to ensure that the net current transferred to the tissue lies within the acceptable range, an additional trimming system is included.

The trimming mechanism allows to fine-tune the currents produced by the sources to minimize the difference in their outputs. To perform this adjustment, a calibration routine must be carried out by the CPU. In this process, a stimulus of a known amplitude and duration is generated by one of the sources and the inverse pulse is replicated in the second source. By means of the additional module proposed in this work, the difference between the output currents is measured. The CPU then verifies whether this difference is acceptable or needs to be corrected. A resulting error higher than the admissible threshold requires that the calibration process be repeated adjusting the trimming bits.

The following chapters focus on the characterization of the existing programmable current sources and the design of the new additional module for precise current adjustment.

Part 2

Characterization of the Integrated Programmable Current Sources

2.1 Introduction

This project is conceived as a part of an existing research initiative from the Microelectronics Group at the Universidad Católica del Uruguay. Two versions of an integrated programmable current source have been designed and fabricated [21] [20] since 2018. The second version was implemented to improve the response time, current consumption and output voltage range achieved in the first version.

In this section, both versions of the existing integrated programmable current sources are characterized and the results are presented.

2.1.1 Current Sources

The initial requirements for the current sources were set with the guidelines given by the company Integer [12].

2.1.1.1 Requirements

The current sources should be capable of delivering or extracting currents in the range of hundreds of µA up to 25 mA. It was determined that 8 control bits would be used for this purpose, allowing to program 256 different values for the output current.

It is also specified that the steady-state output current should remain within ±5% of its target value at all programmable levels. Moreover, the difference between the sourcing and sinking currents must be less than 1 % of their nominal value in each stimulation cycle.

In order to power up the device, there are two main Direct Current (DC) voltage sources required: a Low Voltage (LV) source (3.3 V) and a High Voltage (HV) source (10 V).

The 3.3 V source (V_{DD}) is used to switch on the LV and digital components. The requirement is for the current source to function properly while the output of the LV source remains between 2.8 V and 3.3 V.

The second external voltage source (V_H) is required to supply 10 V. Given the resistance of the ETI and the intensity of the current pulses, it is estimated that under normal circumstances a maximum 9.5 V voltage drop will be produced across the tissue. The voltage drop given by the current sources should be less than 0.5 V, obtaining a maximum voltage difference of 10 V which is limited by the technology.

The specifications state that the device must function correctly with the HV source's output ranging anywhere from 7 V to 10 V.

Additionally, the current source must be capable of performing the stimulation accurately for output voltages (as defined in Figure 3) within 0.5 V-9.5 V, provided that the tissue resistance allows it.

Regarding the current consumption requirements, the specification is to attain efficiencies of over 90%. While this requirement can be flexible for the lower current values, it is especially important for the higher output currents. The efficiency is computed as indicated in Equation 1 where I_{OUT} is the output current and I_V is the total current being drained from the power supply. When the sources are disabled, the current consumption should be less than 1 µA.

$$\text{Efficiency}(\%) = \frac{I_{OUT}}{I_V} \cdot 100 \tag{1}$$

As for the timing requirement, the response time for all programmable current levels must remain under 1 µs.

Additionally, the prototype of the current sources has to fit inside a mini Application-Specific Integrated Circuit (ASIC) block with an area of 1.52 mm x 1.52 mm (2.31 mm^2).

While the prototype will include a single set of sourcing and sinking current sources, a commercial product may integrate multiple sets of current sources. The initial specifications require a minimum crosstalk charge between the different channels (on the order of nC).

The requirements are summarized in Table 1.

Parameter	**Target Range**
Output range	0 - 25 mA
Output precision	$\leq 5\%$
Source difference	$\leq 1\%$
LV supply range	2.8 - 3.3 V
HV supply range	7 - 10 V
Output voltage range	0.5 - 9.5 V
Efficiency	$\geq 90\%$
Response Time	≤ 1 µs
Area	$\leq 2.31\,mm^2$

Table 1: Outline of the specifications for the current stimulator.

2.1.1.2 Design Characteristics

The current sources were designed following the requirements given in section 2.1.1.1 (Requirements). In this section, the design characteristics of both versions are presented.

Both designs were implemented using XFAB's 180 nm CMOS HV technology (XH018) [22]. This allows for the use of 180 nm transistors and HV transistors that can handle up to 200 V with isolation in a Silicon-On-Insulator (SOI) wafer with oxide trenches. Both versions of the current source use transistor from the Primitive Library. The ne3 and pe3 models were used for the LV transistors as

they can withstand a gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) between $-3.6\,V$ and $3.6\,V$. The nmma and pmma transistors are used for the HV design since V_{GS} and V_{DS} can range from $-10\,V$ up to $10\,V$.

Both versions fit inside a mini ASIC block. The area used in the first and second version is $1.11\,mm^2$ and $1.15\,mm^2$, respectively (the area of the CPU is not included).

The output of the first version of the current source can range from $97.7\,\mu A$ to $25\,mA$ with a step size of $97.7\,\mu A$. The second version has a step size of $100\,\mu A$ and thus the output can vary between $100\,\mu A$ and $25.5\,mA$.

In order to achieve the required precision for the output and the current difference, a trimming mechanism was implemented in both versions. As shown in Figure 3, there are additional control bits used to program the trimming mechanism. The working principle of the fine-tuning circuit is presented in section 9.4 (Design of the Current Sources' Trimming Mechanism).

The first version of the current source is designed so that every programmable output for the sinking source can be adjusted more accurately using an additional six trimming bits. The second version implements a symmetrical trimming mechanism on both internal sources. In this case, five trimming bits can fine-tune every output level of each source, also allowing a wide and precise range of currents. Both versions are designed so that setting these trimming bits can reduce the difference in current between both internal sources to under 1 % in each stimulation cycle. To control these bits, a RISC-V processor working at 3.3 V is used.

Aside from the LV and HV voltage sources, a current source (I_{BIAS}) is required. The first version of the current stimulator takes a 50 nA current input whereas the second version is designed for a $1\,\mu A$ input. The second version also requires the addition of two external voltage sources with values $9.4\,V$ ($V_H - 0.6\,V$) and $0.6\,V$ ($GND + 0.6\,V$). These additional inputs are included in the prototype, however, a final design would generate them internally. Figure 4 represents the input and output diagram for both versions of the current source.

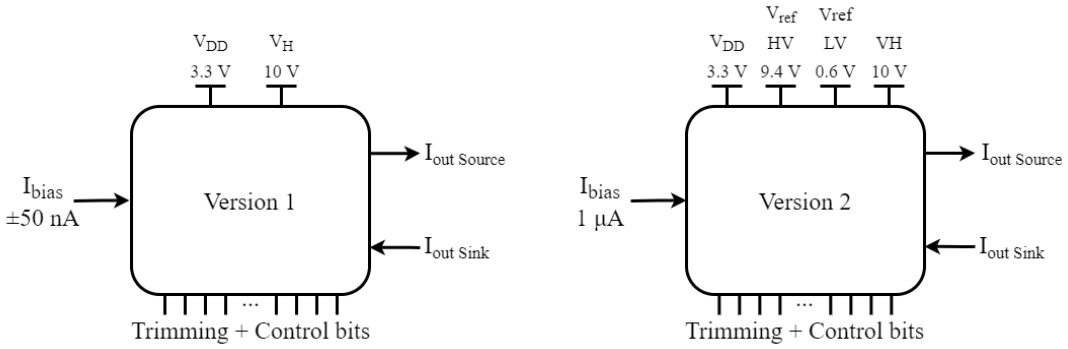

Figure 4: Diagram showing the inputs and outputs for both versions of the integrated programmable current stimulator.

2.2 Measurements

A complete characterization of both versions of the current source includes measurements of all of the electrical parameters referred to in section 2.1.1 (Current Sources).

The following subsections present the setup used for the measurements as well as the results obtained. This includes the characterization of the current output range for both internal sources, the trimming system, response times and current consumption. It also shows the experimental output current range as the voltage and current inputs (V_{DD}, V_H and I_{BIAS}) and the output voltage are swept.

2.2.1 Setup

2.2.1.1 First Version

For the first version of the current source 15 chips were manufactured and 7 of them were encapsulated as shown in Figure 5.

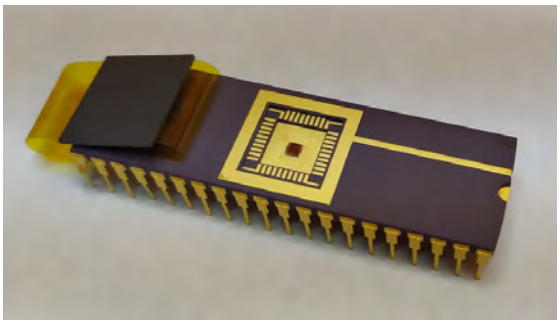

Figure 5: Photograph showing the chip of the first version manufactured with its packaging (from Reference [20]).

A custom Printed Circuit Board (PCB) was designed to test the current source and other circuits integrated in this chip (Figure 6).

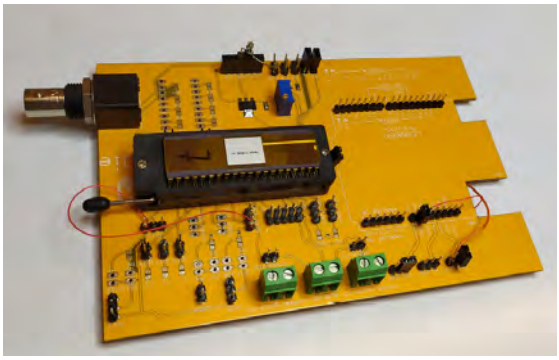

Figure 6: Photograph of the PCB designed to test the first version of the chip (from Reference [20]).

Additionally, the following equipment was used to implement the measurement setup for the first version of the current source:

- A 10 VDC and a 3.3 VDC voltage source.
- A current source or Source Measure Unit (SMU) capable of supplying a 50 nA current.
- An SMU capable of supplying voltages up to 10 VDC and with a current limit of over 25 mA. This SMU is connected at the output and simulates the voltage drop across the tissue. A set of resistors can also be used to simulate the tissue as the output current is swept.
- An external Microcontroller Unit (MCU) with at least 5 General-Purpose Input/Outputs (GPIOs) available, driven by 3.3 VDC.
- A multimeter (ammeter) capable of measuring currents up to 25 mA with a precision of at least 1 µA.
- An oscilloscope with a bandwidth of at least 10 MHz.

The general setup used in the characterization process is depicted in Figure 7. To test only the sinking current source, the IBIAS_SINK input from Figure 7 must be connected to the 50 nA current but IBIAS_SOURCE may remain unpowered and vice versa.

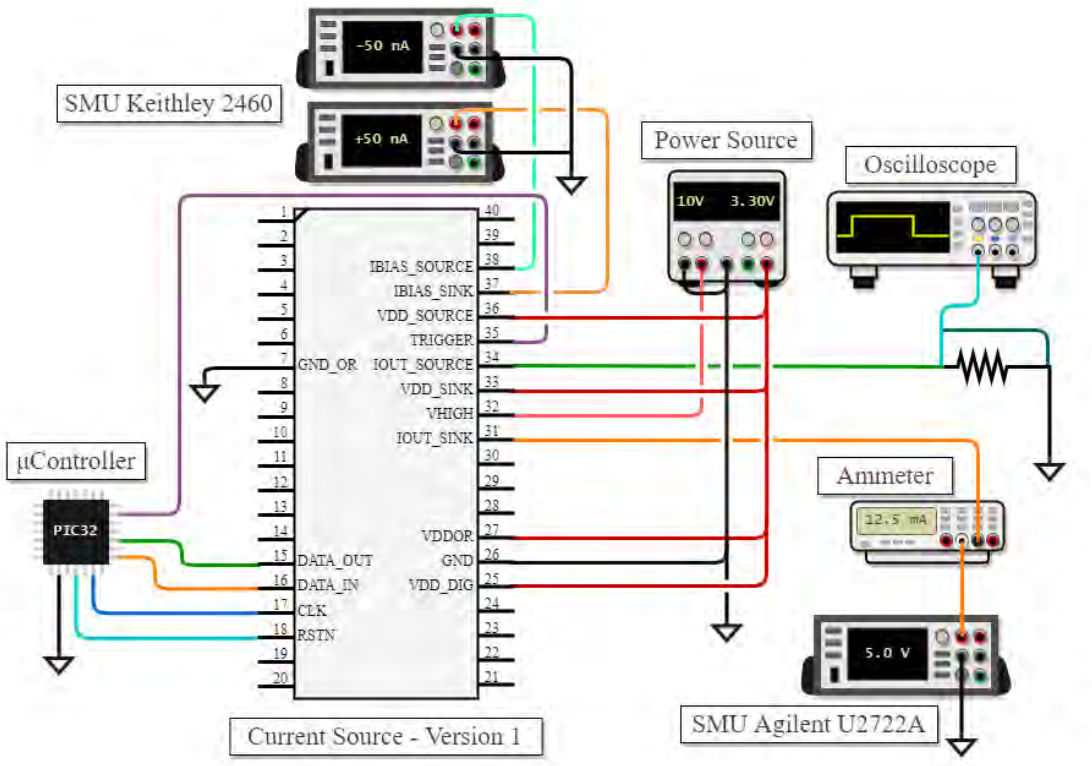

Figure 7: Setup for the characterization of the first version of the integrated programmable current source.

As shown in the diagram, the output being measured may be connected to an SMU to simulate the voltage drop across the tissue. An ammeter may also be needed depending on the precision of the SMU as indicated for the IOUT_SINK output in the diagram. For other parameters, such as the response time, an oscilloscope is necessary to measure the output. In this case, a set of resistors can also be used to simulate the voltage drop across the tissue and the current can be computed by measuring that voltage drop. This is shown in Figure 7 for the IOUT_SOURCE output.

On the other hand, an external MCU was used to implement the program that sets the output current and the duration of the pulses. This MCU is used to simulate the internal RISC-V processor. The programming bits to select the current level and the enable bits are loaded into a shift register. The clock and reset signal are also generated along with the trigger signal that initiates the stimulation. The firmware implemented to test the current source is presented in section 9.2 (Firmware for the Microcontroller).

The PCB was placed inside a Faraday's cage to block Electromagnetic Interference (EMI) while taking the measurements.

2.2.1.2 Second Version

For the second version of the current source, 10 samples were manufactured in the same die as the CPU. A QFN package with 80 pins was used (Figure 8) as more inputs and outputs were needed for this version. A new custom PCB (shown in Figure 9) was designed in this project to test the chip. The schematic and board are shown in section 9.3 (PCB for the Second Version of the Current Source).

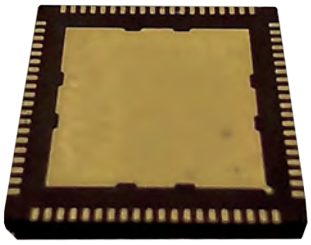

Figure 8: Photograph of the QFN package with the second version of the chip.

The following equipment was used to characterize the second version of the current source:

- A 10 VDC, a 3.3 VDC, a 0.6 VDC and a 9.4 VDC voltage source.
- A current source or SMU to supply a 1 µA current.
- An SMU capable of supplying voltages up to 10 VDC with a current limit of over 26 mA. This SMU is connected at the output and simulates the voltage drop across the tissue. A set of resistors can also be used for this purpose.
- An external MCU with at least 5 GPIOs available, driven by 3.3 VDC.

Figure 9: Photograph of the PCB designed to test the second version of the chip.

- A multimeter (ammeter) capable of measuring currents up to 26 mA with a precision of at least 1 µA.
- An oscilloscope with a bandwidth of at least 10 MHz.

Just as with the first version, an external MCU was used to implement the program that sets the output current and the duration of the pulses. This MCU is used in place of the internal RISC-V processor so as to test the current source independently.

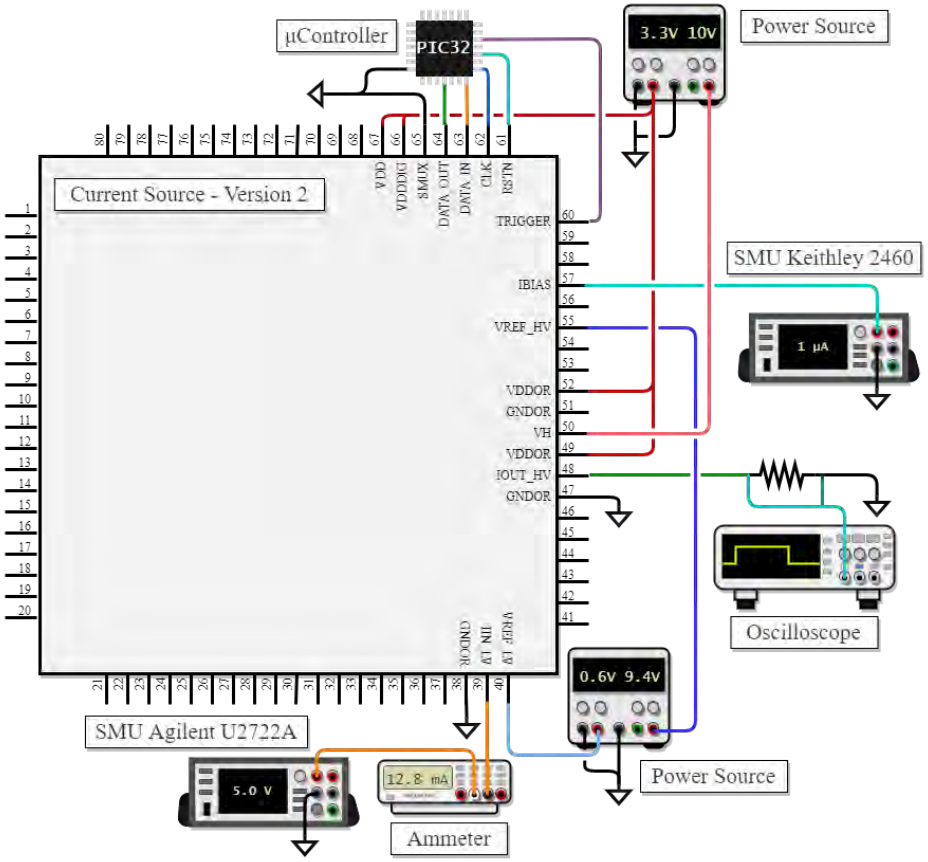

Figure 10: Setup for the characterization of the second version of the integrated programmable current source.

The general setup for the characterization of the second version of the chip is depicted in Figure 10 and it is similar to that of the first version presented in Figure 7.

Besides the difference in the trimming mechanism of both versions, there is also a slight difference in the structure of the shift register. Thus, the way the programming bits and trimming bits are loaded was modified in a new version of the firmware implemented for the external MCU as can be seen in section 9.2 (Firmware for the Microcontroller).

2.2.2 Results

In this section the results of the characterization for both versions of the current source are presented and contrasted. Each measurement was repeated on at least two different chips and compared against the requirements.

2.2.2.1 Bias Current - Output Current Relation

In order to obtain the bias current - output current relation, the SMU is connected to the bias current input and swept. All other parameters are kept at their nominal values and the output current is measured using the SMU or an ammeter.

The results for the first version of the current source are plotted in Figure 11. It can be seen that the bias current - output current relation is mostly linear as is expected from the design. The non-linearity when sinking current is also expected due to the saturation of the components.

Another aspect to note is that the measured and the designed operating points differ for both sources. This difference is even more noticeable when the chip is sourcing current. It was found that the cause of this effect detected through the measurements is related to the pad used for the bias current input. The documentation [23] for model AP3VLR15BF specifies that the maximum pad voltage for a low leakage current is 3.6 V. Instead, a voltage of around 8 V was measured at the input during the testing phase. As can be seen in Figure 13, the documentation shows that the pad's leakage current at 8 V is approximately 50 nA. As a consequence, most of the input bias current leaves the pad through the Electrostatic Discharge (ESD) protection cell. This explains why the operating point when sourcing is shifted by over 50 nA. In the case of the sinking source, the voltage at the pad is lower than 3 V and the leakage current through the AP3VLR15BF is of around 30 pA. This is negligible compared to the 50 nA bias current and consequently the sinking source is affected differently.

To fix this issue, the bias current input was adjusted by the measured offset in the operating point and was corrected for all of the subsequent measurements.

The measurements were repeated on the second version of the current source (Figure 12). Unlike the first version, the measured and designed operating points are close enough to validate the design. Since in this case a 1 µA current was used, the effect caused by the pads in the first version was not detected here.

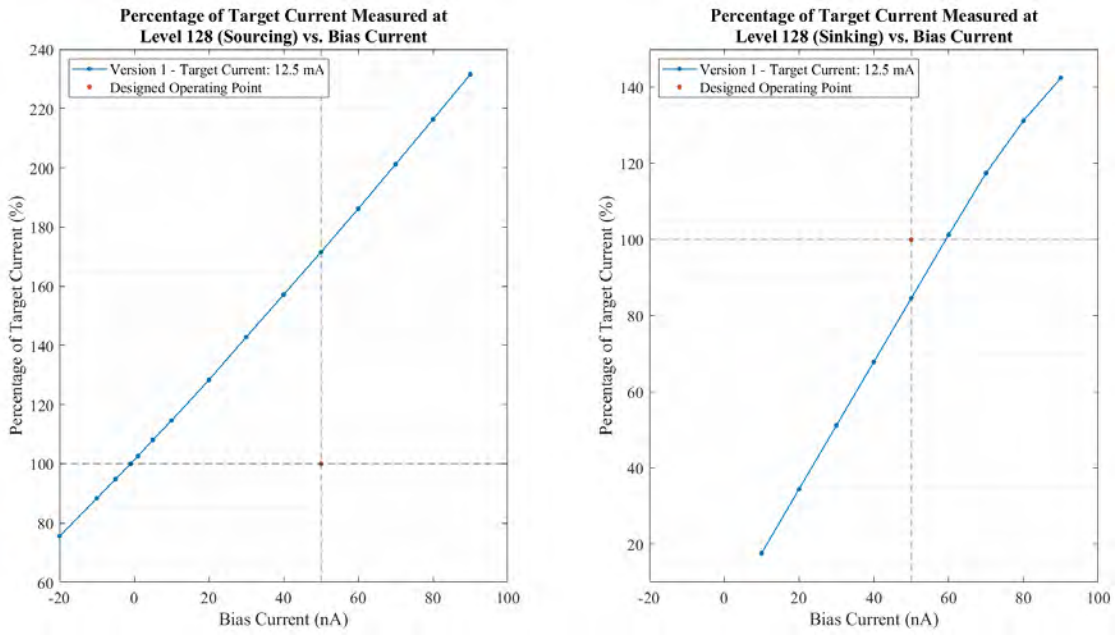

Figure 11: Plot of the percentage of target current achieved for the first version of the current source against the bias current. The operating point for which the current source was designed is indicated in orange. The measurements were taken with the output programmed at level 128.

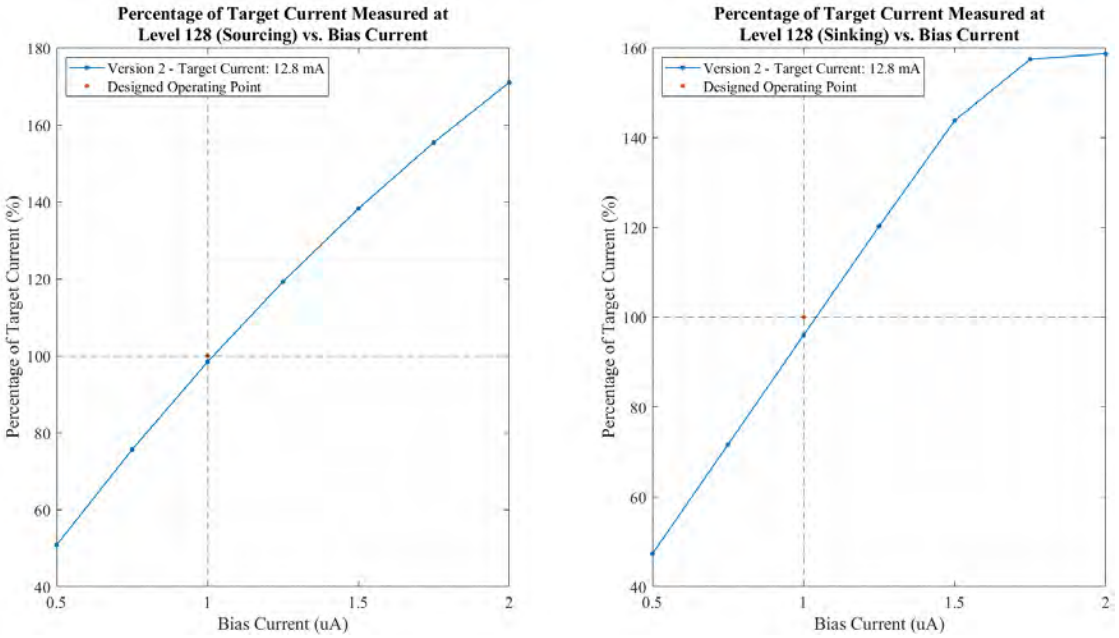

Figure 12: Plot of the percentage of target current achieved for the second version of the current source against the bias current. The operating point for which the current source was designed is indicated in orange. The measurements were taken with the output programmed at level 128.

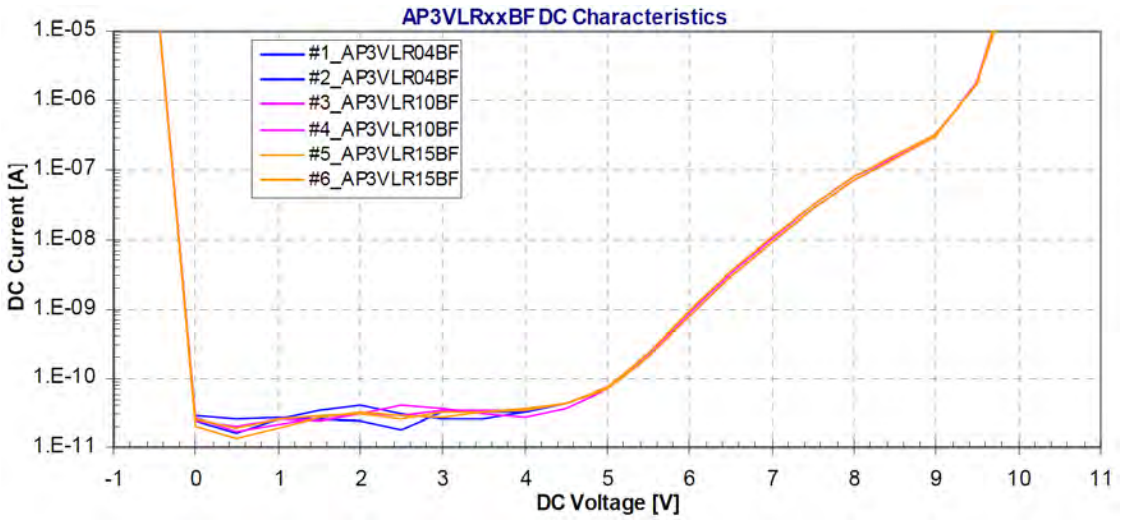

Figure 13: Plot of the leakage current through pad AP3VLR15BF used for the bias current input in the first version of the chip against its DC voltage. The image was extracted from Reference [23].

2.2.2.2 Output Current Range

In order to characterize the output current range, all 255 levels were programmed and measured using the ammeter. The trimming bits were kept fixed at their nominal values.

The results for the first and second version are presented in Figure 14 and Figure 15, respectively, where the achieved current range is displayed.

A more detailed plot is shown in Figure 16 and Figure 17. The current output is plotted as the percentage of the target current for each level along with the lower and upper bounds set in the specifications.

It can be seen from the plots that for most levels, the output current is within the specified 5% margin. For the cases where the output differs considerably from the designed nominal value, the trimming system can be applied. This is explored in section 2.2.3 (Simulated Trimming Model for Current Adjustment).

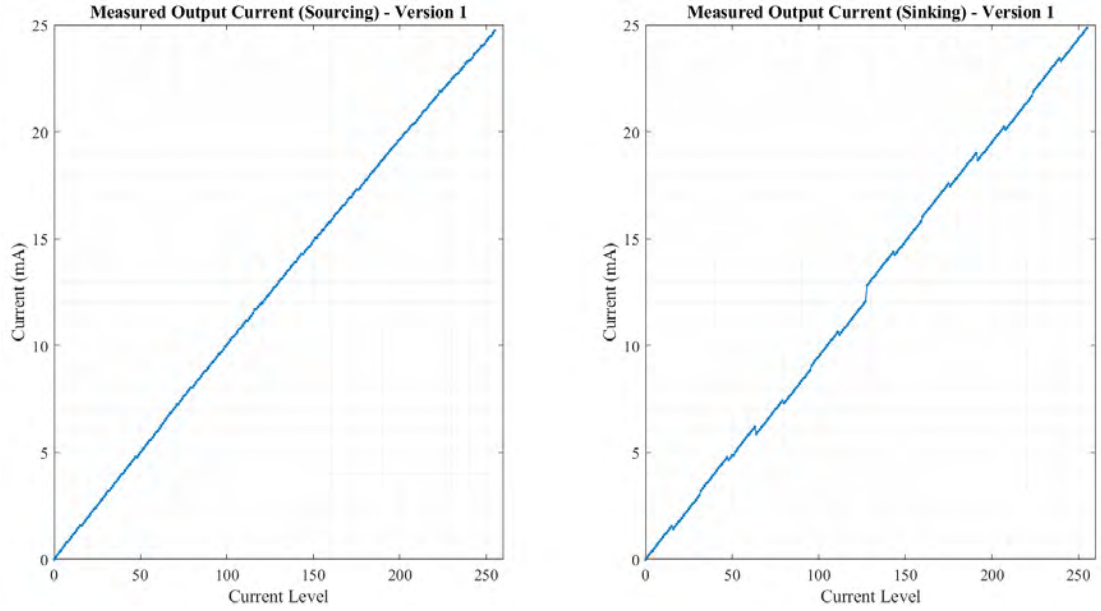

Figure 14: Plot of the output current against the current level for the first version.

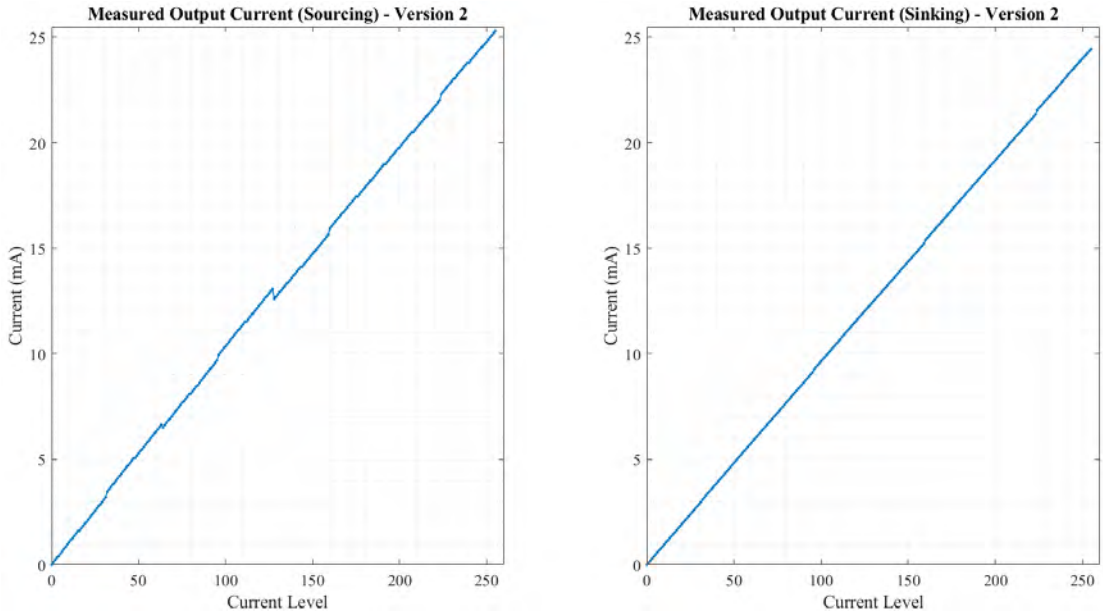

Figure 15: Plot of the output current against the current level for the second version.

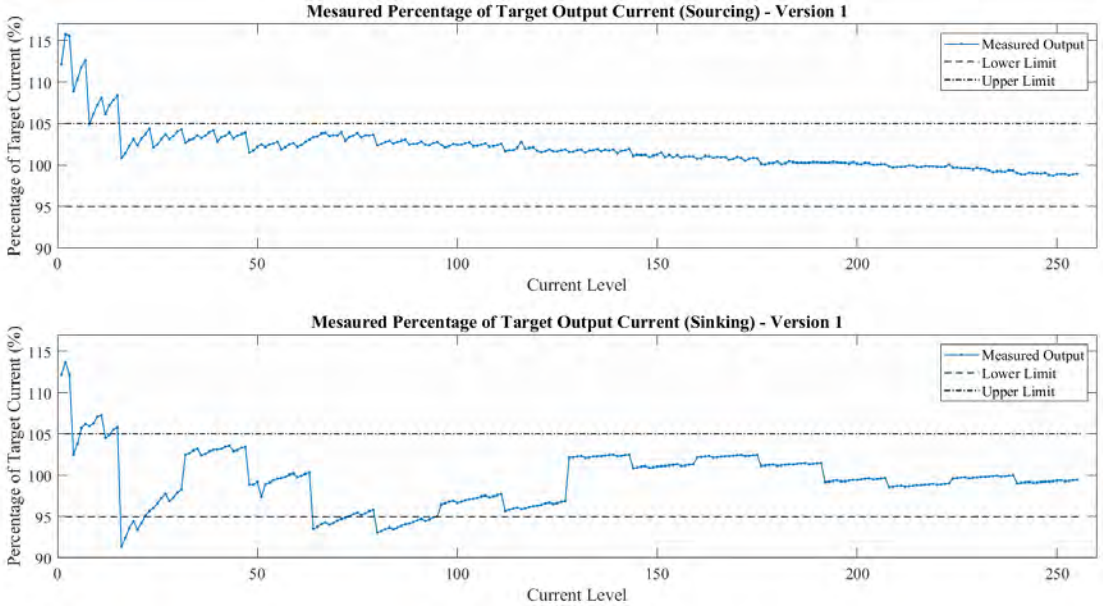

Figure 16: Plot of the measured percentage of target current for the first version.

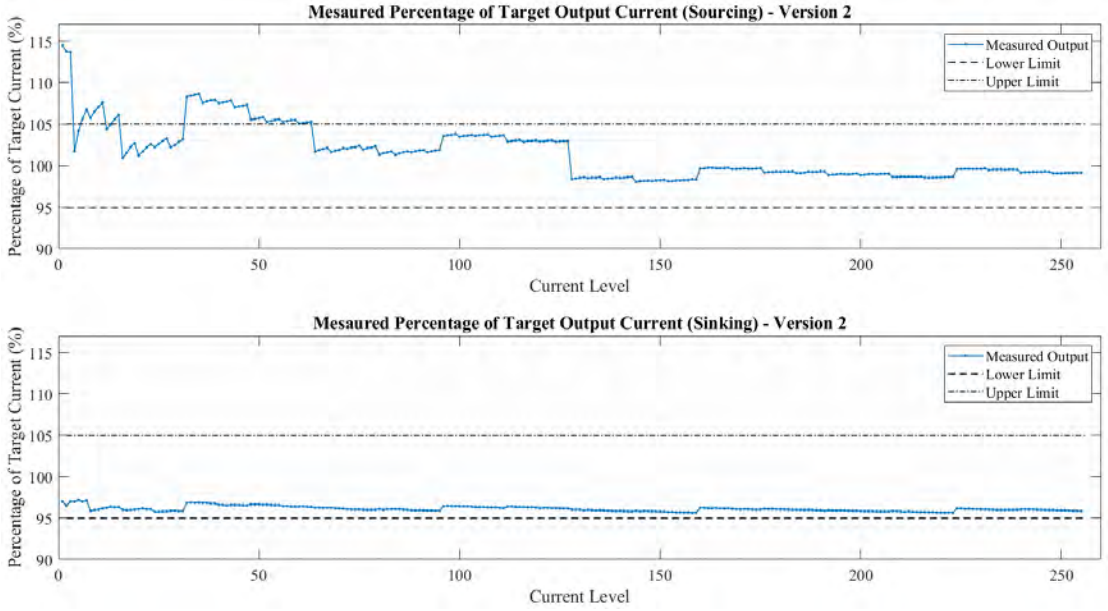

Figure 17: Plot of the measured percentage of target current for the second version.

2.2.2.3 Trimming Mechanism

The trimming system allows to precisely adjust the current output as described in section 1.4 (Objective and Framework). The working principle of the trimming mechanism is presented in section 9.4 (Design of the Current Sources' Trimming Mechanism). In order to test it, a current level is set and all trimming values are programmed one at a time. The current output is measured using the ammeter. All other parameters are kept at their nominal values.

The results obtained for the first version of the current source are shown in Figure 18. In this version the trimming system is implemented with 64 levels and is only applied to the source that sinks current. The plots represent the output currents while sinking the maximum and minimum currents for the different trimming levels. Both measured and theoretical currents are plotted together for comparison. The nominal current and its lower and upper bounds are indicated as well as the nominal trimming value.

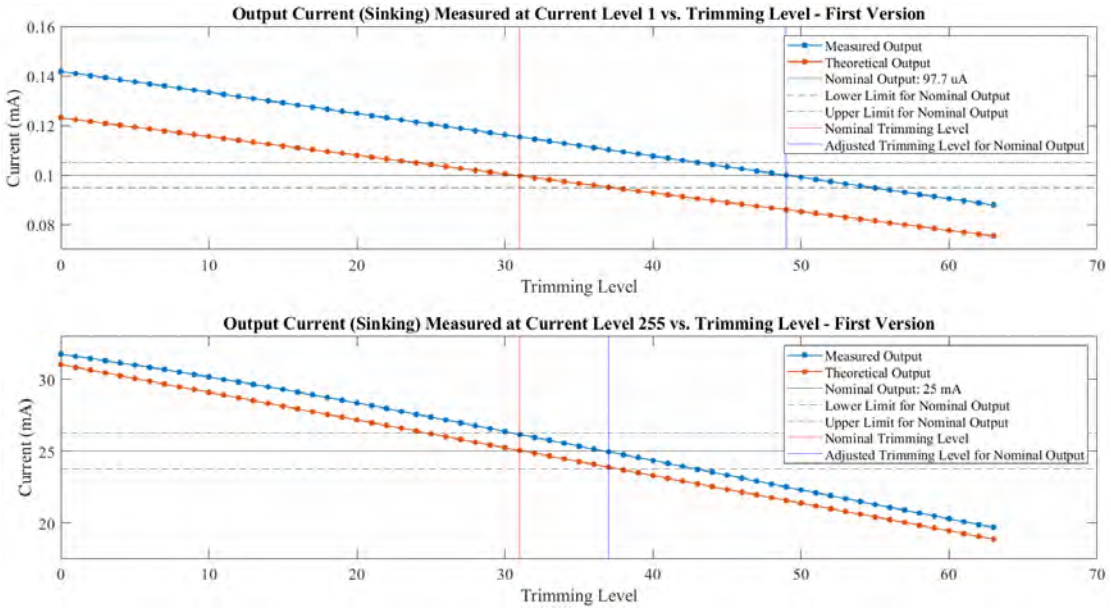

Figure 18: Plot of the output current (sinking) for the first version against the trimming level. The control bits for the output are fixed at both, the maximum and minimum levels.

As can be seen in Figure 18, the trimming system exhibits a linear behavior and is capable of adjusting the current between the acceptable limits despite not matching exactly the theoretical values.

The characterization of the trimming mechanism for the second version is shown in Figure 19 and Figure 20. In this design, trimming can be performed with 32 possible levels while sourcing and sinking current.

As with the first version of the current source, the second version shows a linear behavior. Changing the trimming bits produces a current output between the specified bounds and with the required precision.

2.2.2.4 Supply Voltage Range

To check the supply voltage range, both V_{DD} and V_H power sources are swept independently while all other parameters remain nominal. The output current is measured using the ammeter and plotted in Figure 21. The data collected for both versions is overlapped for comparison and the admissible ranges defined in the specifications are shaded in the plot.

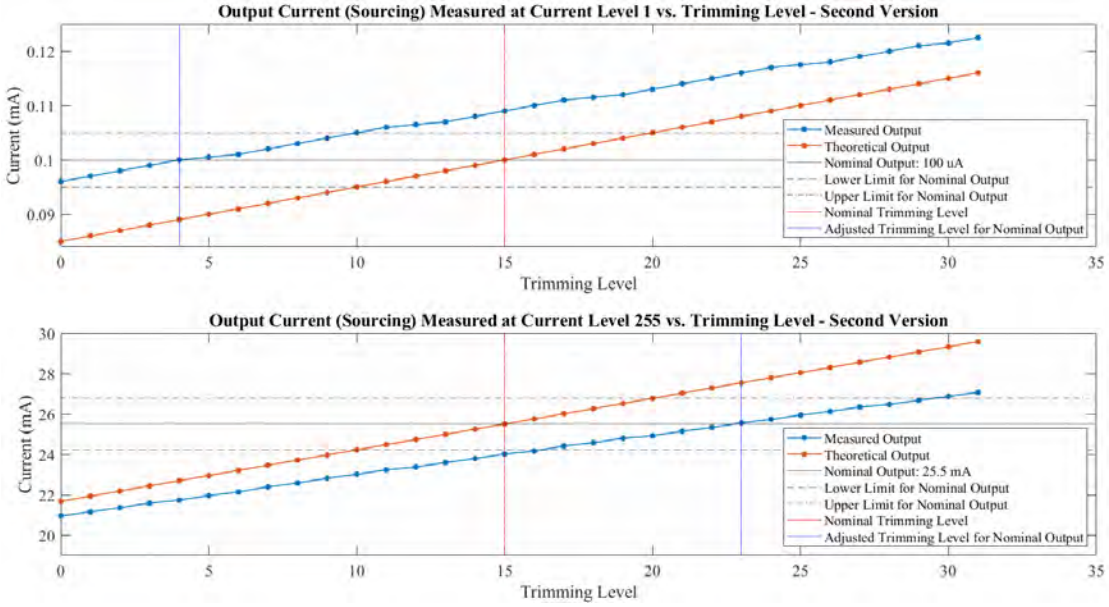

Figure 19: Plot of the output current (sourcing) for the second version against the trimming level. The control bits for the output are fixed at both, the maximum and minimum levels.

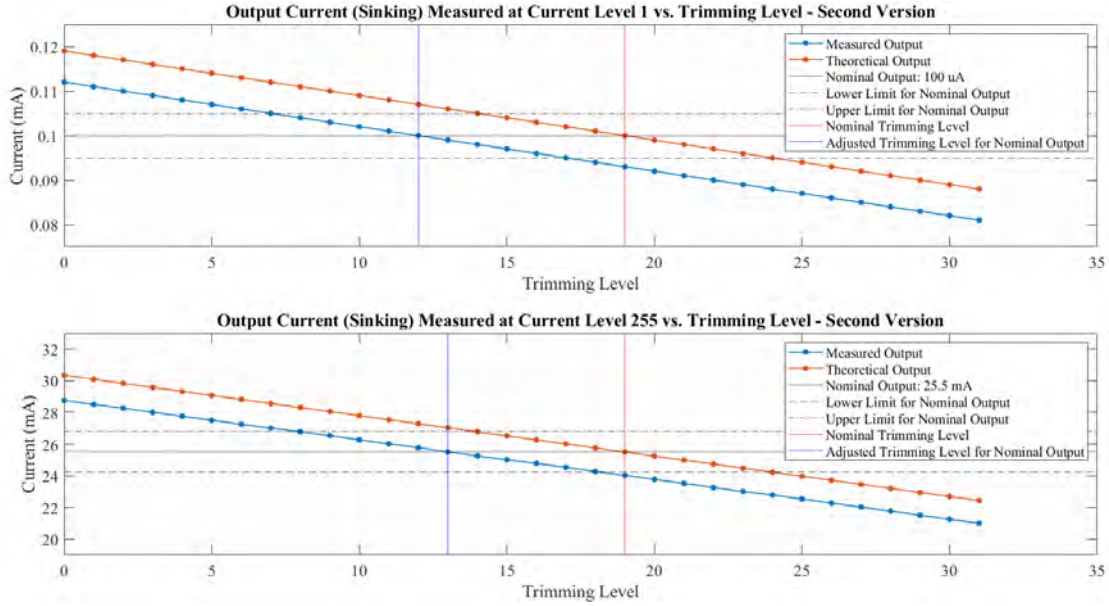

Figure 20: Plot of the output current (sinking) for the second version against the trimming level. The control bits for the output are fixed at both, the maximum and minimum levels.

Figure 21 shows that both versions behave substantially different. In the case of the first version, the specified supply voltage range is not achieved for either V_H or V_{DD}. For the lower voltages in both ranges, the output is well below 95% of the nominal value. In the second version, however, this issue is fixed and the requirements are successfully met.

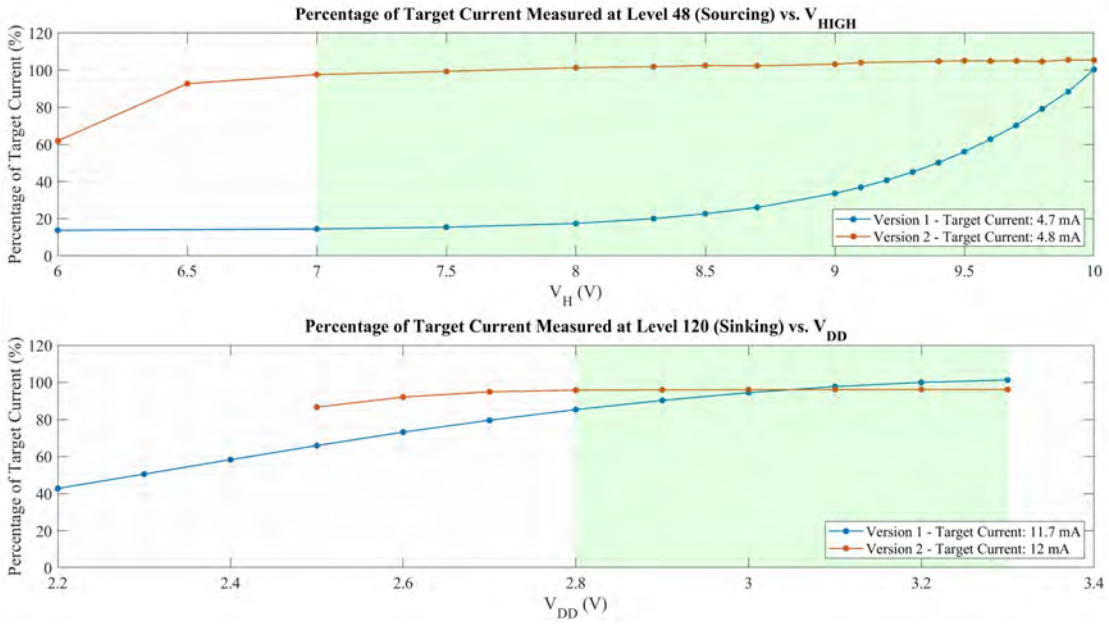

Figure 21: Plot of the percentage of target current achieved for both versions of the current sources against the supply voltage (V_H when sourcing and V_{DD} when sinking). The area shaded in green represents the working requirements.

In the first version, the supply voltage ranges obtained are roughly 3.1 V-3.3 V for V_{DD} and 9.9 V-10 V for V_H. For the second version, these ranges resulted in 2.6 V-3.3 V and 6.7 V-10 V, respectively.

2.2.2.5 Current Consumption

Current consumption measurements were performed on both versions. An ammeter was connected to the 10 V and the 3.3 V power supply to measure the current consumption while sourcing or sinking current, respectively. Table 2 and Table 3 show the average results for multiple current levels programmed on two different chips.

It can be seen from the results that the efficiencies for most levels are above the 90% requirement. The levels for which the efficiencies are significantly lower than 90% correspond to outputs below 1 mA.

It may also be noted that in the second version, the maximum current consumption of the sourcing current source was reduced significantly for the higher levels, reaching a 65% decrease for level 255.

On the other hand, while on the disabled status, the current consumption of the first version is 70 µA and 17 µA for the sourcing and sinking current sources, respectively. For the second version, both values were negligible when measured with a 1 µA resolution ammeter.

Current Level	Version 1 Output Current (mA)	Version 1 Current Consumption (µA)	Version 1 Efficiency (%)	Version 2 Output Current (mA)	Version 2 Current Consumption (µA)	Version 2 Efficiency (%)
1	0.12	84	**59**	0.12	65	**64**
2	0.24	84	**74**	0.23	65	**78**
7	0.82	132	**86**	0.75	65	92
8	0.88	89	91	0.84	65	93
15	1.68	162	91	1.58	65	96
16	1.66	90	95	1.60	130	93
31	3.30	193	94	3.16	130	96
32	3.31	111	97	3.42	130	96
63	6.39	244	96	6.48	130	98
64	6.46	119	98	6.36	130	98
127	12.12	304	98	12.43	130	99
128	12.27	158	99	12.03	130	99
254	22.03	377	98	22.29	130	99
255	22.11	401	98	22.47	130	99

Table 2: Consumption and efficiency while sourcing current with both versions. Efficiencies under 90% are highlighted.

Current Level	Version 1 Output Current (mA)	Version 1 Current Consumption (µA)	Version 1 Efficiency (%)	Version 2 Output Current (mA)	Version 2 Current Consumption (µA)	Version 2 Efficiency (%)
1	0.11	32	**78**	0.09	72	**56**
2	0.22	32	**87**	0.19	72	**72**
7	0.72	51	93	0.68	72	90
8	0.83	32	96	0.76	72	91
15	1.55	60	96	1.44	72	95
16	1.43	32	98	1.53	200	**88**
31	2.99	70	98	2.97	200	94
32	3.20	42	99	3.09	200	94
63	6.19	89	99	6.06	200	97
64	5.87	67	99	6.15	200	97
127	12.06	133	99	12.19	200	98
128	12.81	99	99	12.28	200	98
254	24.77	200	99	24.32	200	99
255	24.88	210	99	24.41	200	99

Table 3: Consumption and efficiency while sinking current with both versions. Efficiencies under 90% are highlighted.

2.2.2.6 Response Times

The response times are obtained using an oscilloscope that measures the voltage drop across a resistor modelling the tissue at the output of the current source. Once the waveforms are captured, the response time is extracted. This is the time that it takes from the start of the trigger pulse until the voltage across the resistor remains within ±10% of its steady-state value. Figure 22 indicates the response time and the input and output waveforms generated for the second version of the current source using current level 8. The measurements are repeated across two different samples and then averaged.

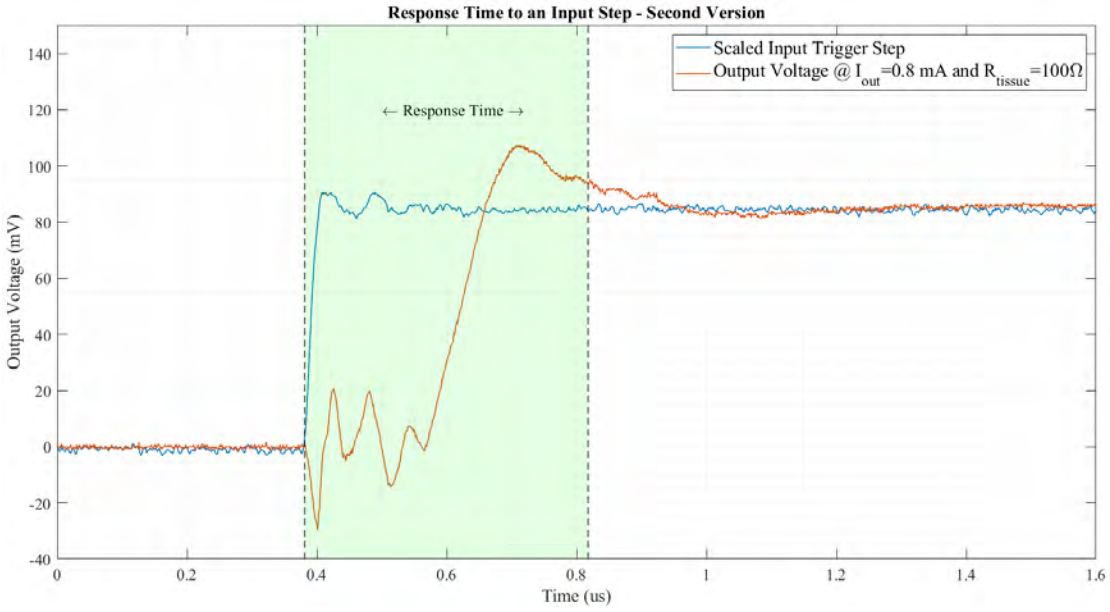

Figure 22: Response time for the second version of the current source measured at an output current level 8 and a tissue resistance of 100 Ω. The scaled trigger pulse is indicated along with the output voltage pulse generated.

Table 4 shows the results for multiple current levels on both versions of the current source.

Some of the response times for the first version are much higher than the 1 µs specification (reaching almost 3.5 µs when sourcing the highest current). The second version was designed to improve these response times. The measurements show that the new version meets the requirement for all of the levels that were tested.

Current Level	Response Times (µs)			
	Sourcing		Sinking	
	Version 1	Version 2	Version 1	Version 2
1	0.563	0.961	**1.165**	0.913
2	0.537	0.641	**1.214**	0.700
8	0.256	0.437	0.902	0.446
15	0.513	0.550	0.901	0.452
16	0.244	0.380	0.956	0.456
32	**1.240**	0.425	0.751	0.480
64	**1.615**	0.508	0.492	0.524
128	**1.773**	0.643	0.485	0.752
255	**3.477**	0.926	0.665	0.972

Table 4: Response times for multiple current outputs measured on both versions of the current source. Results that are over the 1 µs requirement are highlighted.

2.2.2.7 Output Voltage Range

The output voltage range is measured by sweeping the voltage provided by the SMU simulating the tissue at the output of the current source.

Figure 23 shows the output voltage characteristic for both sources and versions. The measurement was performed for the intermediate level 128. The target range is also represented by the area shaded in green.

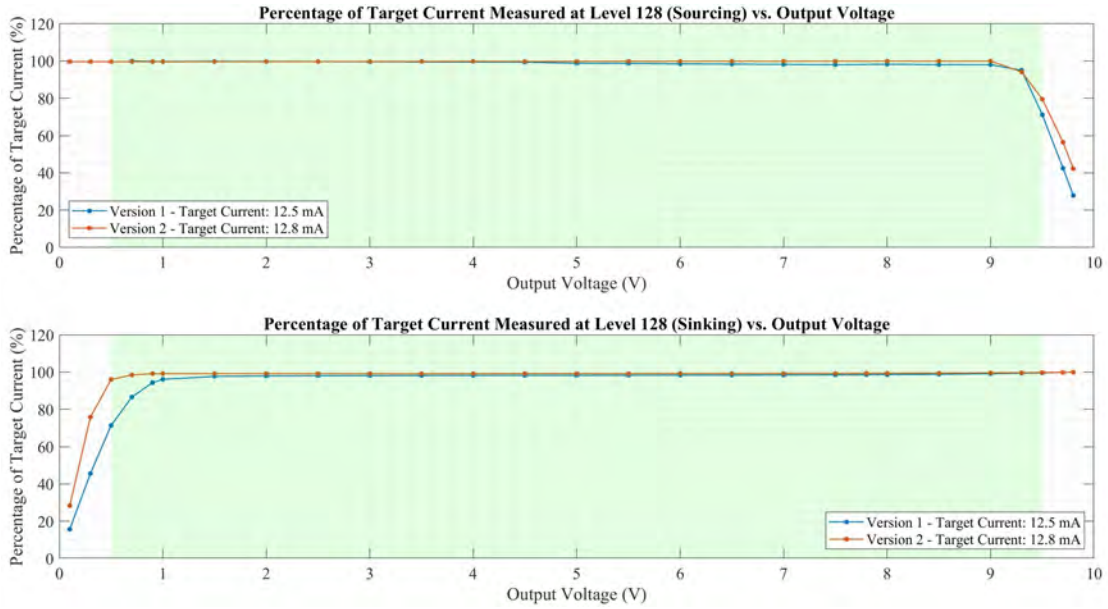

Figure 23: Plot of the percentage of target current achieved against the output voltage for both versions of the current sources. The area shaded in green represents the working requirements.

The plot shows that the output voltage range is 0.9 V-9.3 V for the first version and 0.5 V-9.2 V for the second version. Both are slightly off compared to the required 0.5 V-9.5 V range.

2.2.2.8 Crosstalk

Crosstalk is the defined as the charge delivered to an electrode through an ideally open circuit while another channel is stimulating the tissue. This parameter is particularly relevant for an application that includes several current sources in the same Integrated Circuit (IC). As mentioned in section 2.1.1.1 (Requirements), a crosstalk charge on the order of nC is considered acceptable [20].

The resulting crosstalk is measured by sensing the output current on the source that is not activated. Thus, when the stimulator is sourcing current, the output of the sinking source is measured and vice versa. To obtain the current vs. time plot, the oscilloscope is used to measure the voltage drop across a resistor modelling the tissue. The current is then calculated and numerically integrated in time to compute the crosstalk charge.

The measurements were performed for output levels 128 and 255 since for the lower currents this effect was negligible. The results are presented in Table 5 where data was collected for two different chips and averaged.

On mode	**Current Level**	**Crosstalk Charge (pC)**			
		Sourcing		**Sinking**	
		Version 1	**Version 2**	**Version 1**	**Version 2**
Sourcing	255	-	-	6560	4.68
	128	-	-	3738	2.77
Sinking	255	11.98	0.70	-	-
	128	6.61	0.34	-	-

Table 5: Total charge delivered from the crosstalk currents measured on both versions.

It can be seen that crosstalk is reduced considerably in the second version of the current source where all values are in the pC range.

2.2.3 Simulated Trimming Model for Current Adjustment

As indicated in section 2.2.2.2 (Output Current Range), the fine-tuning mechanism may be used to adjust the current output when it differs from the nominal value. Not only can it fix the steps with higher errors but it may also be used to eliminate the scattered lack of monotonicity in the outputs shown in Figure 14 and Figure 15.

Using the data collected by the measurements from the current outputs and the trimming system in section 2.2.2.2 (Output Current Range) and section 2.2.2.3 (Trimming Mechanism), an adjusted current output was computed for all levels of the second version of the current source.

Starting from the experimental output current measured at the nominal trimming level, the adjusted trimming level was computed. This level sets the output current closest to its target value. The calculation was done by considering a trimming step size of 0.92% of the nominal current output (instead of the theoretical value

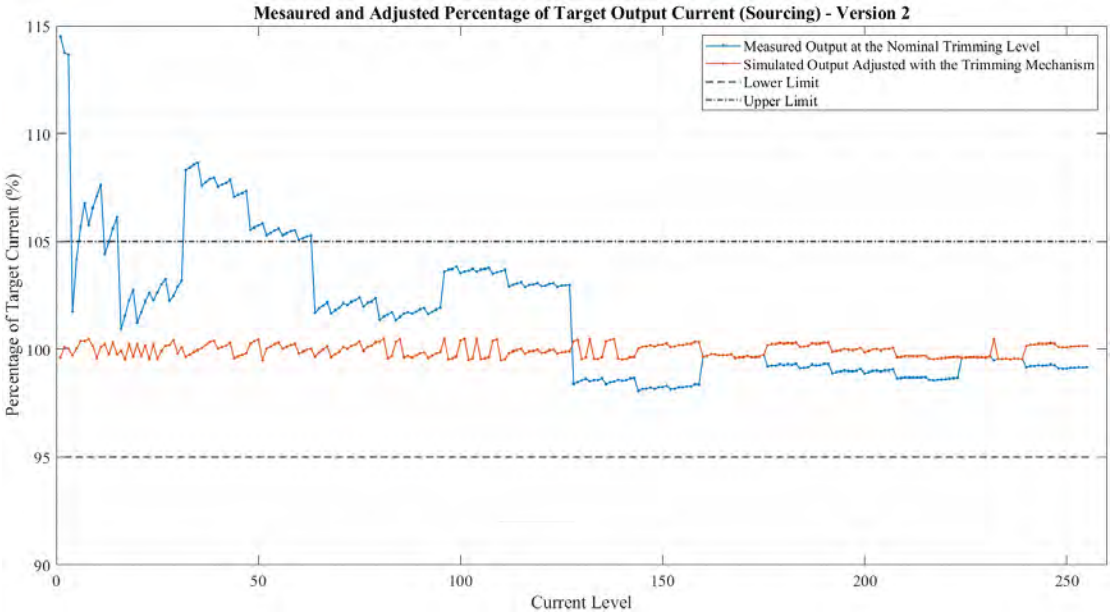

Figure 24: Plot of the measured percentage of target current while sourcing all outputs at the nominal trimming level (blue) and the percentage that can be obtained by changing the trimming bits to their optimal value (orange).

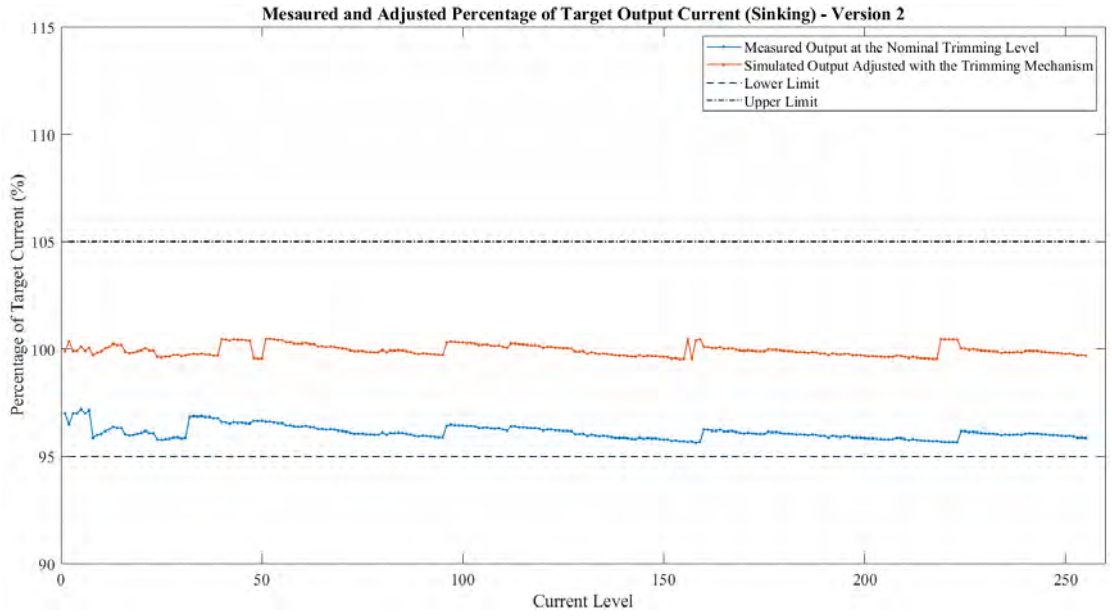

Figure 25: Plot of the measured percentage of target current while sinking all outputs at the nominal trimming level (blue) and the percentage that can be obtained by changing the trimming bits to their optimal value (orange).

of 1%) which was the average obtained for ten different sets of measurements. Taking the known nominal trimming level and the percentage difference in the measured and nominal output currents, the ideal trimming level was calculated in each case.

The results are shown in Figure 24 and Figure 25 where the output is presented as a percentage of the nominal (target) current. The measured and the adjusted output currents are overlapped for comparison.

It can be seen from both plots that it is always possible for the output to remain within a ±1% of the target value when trimming is performed. This also confirms that the specifications for the output accuracy and output source difference in Table 1 are met.

2.3 Conclusions

The measurement process and analysis of the data collected has allowed to validate the design, identify issues and highlight the improvements achieved in the second version of the current stimulator.

Table 6 presents the resulting design specifications for both sources along with the target ranges defined in the requirements as indicated in Table 1.

As shown in Table 6, the second version of the current source meets most of the requirements while improving the output current range and accuracy, the source difference, the response times, and the output and supply voltage ranges.

Parameter	**Target Range**	**Version 1**	**Version 2**
Output range	0 - 25 mA	0 - 25 mA	0 - 25.5 mA
Output precision	<5%	<5%*	<1%**
Source difference	<1%	<2%**	<1%**
LV supply voltage range	2.8 - 3.3 V	3.1 - 3.3 V	2.6 - 3.3 V
HV supply voltage range	7 - 10 V	9.9 - 10 V	6.7 - 10 V
Output voltage range	0.5 - 9.5 V	0.9 - 9.3 V	0.5 - 9.2 V
Efficiency	>90%	>94%***	>94%***
Response Time	<1 us	<3.48 us	<0.97 us
Area	<2.31 mm^2	1.11 mm^2	1.15 mm^2

Table 6: Measurement results for both versions and the target values set in the specifications. Results that fall within the requirements are indicated in green, otherwise they are marked in red. *For current levels over 15. **Applying the trimming mechanism. ***Efficiencies for higher currents (over 2 mA).

Part 3

Design of the Calibration Module

This section presents the schematic design of an additional module to improve the existing current stimulator. The purpose of this calibration module is to detect possible current differences between the internal sources when the stimulation is performed. This would allow to adjust the trimming levels and correct the current mismatch if required.

3.1 Introduction and Initial Requirements

As mentioned in section 1.2.1 (Charge Balance and Current Stimulators), a practical way of verifying that the biphasic stimulation pulses are charge-balanced is by maintaining a current difference between the sourcing and sinking phases below 1%. The purpose of the calibration module is to measure this difference which is then compared against the threshold in the CPU. If necessary, the CPU will apply the corrections to the sources using the trimming mechanism based on the measurement received from the module. Besides this current adjustment, no timing corrections are performed since this can be precisely controlled by the CPU. Additionally, the rise and fall times for the pulses are orders of magnitude lower than the stimulation times.

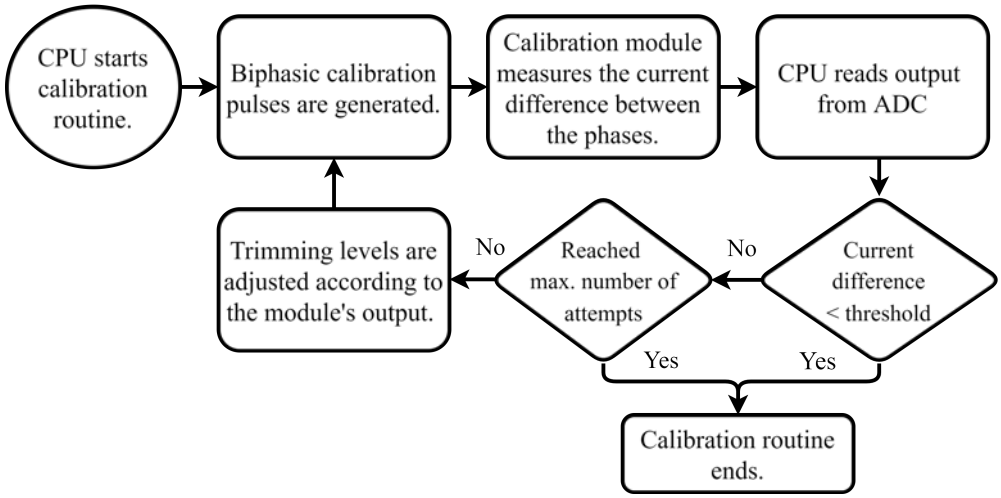

Figure 26: Flowchart showing the sequence of steps for the calibration routine.

The designed calibration system follows the sequence shown in Figure 26. First, the calibration routine is initialized by the CPU and a calibration biphasic pulse of a given duration is generated. This pulse should have the desired amplitude for the subsequent stimulations of the tissue. The calibration module then takes the necessary measurements to evaluate the difference in output currents between both phases of the stimulation pulses. The output of the calibration module is connected to an input of the CPU which compares the result against the threshold. If validated, the calibration process is completed without modifications to the trimming levels. Otherwise, the trimming levels are adjusted accordingly and another sequence of the calibration process is performed until the difference is acceptable or until a defined maximum number of calibration routines is performed.

The calibration process may be carried out every time the stimulation amplitude is modified or periodically to ensure that the charge balance still holds.

It is required for the calibration module to have an analog output related to the current difference being measured. The diagram for the new version of the stimulator with the addition of the calibration module is shown in Figure 27.

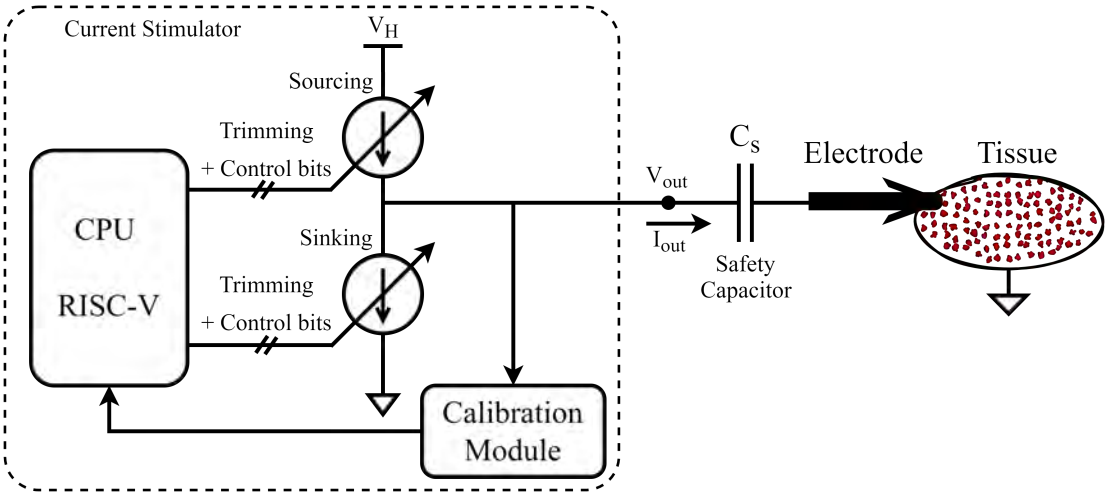

Figure 27: Simplified diagram for the current stimulator with the calibration module.

The input of the calibration module, i.e., the node where the current difference will be measured from, is the output of the current source as illustrated in Figure 27.

The measurement process performed by the calibration module has to be done efficiently and without affecting the stimulation current or voltage. The module has to be capable of being added to the existing current stimulator, namely the second version of the current source, without modifying it internally.

The initial requirements are summarized in Table 7. The input is an analog signal that can range from 0 to 5 V.

Parameter	**Target Range**
Output	Analog LV output related to the current difference
Input	Analog input in the 0 - 5 V range
Area	Less than 30% of the area of the current source
Timing	The duration for the calibration pulse should be in the 10 µs - 10 ms range

Table 7: Initial design requirements for the calibration module.

The output is also a LV analog signal related to the current difference. It will be connected to a 12-bit Analog-to-Digital Converter (ADC) inside the processor (if necessary, through an amplifier or a voltage divider).

As for the time requirements, the duration of the calibration pulse should not exceed 10 ms which is the limit defined for the stimulation.

The area of the module should be less than 30% of the total area of the current sources. In the case of the second version of the current source this implies a maximum area of roughly $0.345\,\mathrm{mm}^2$.

3.2 Output Voltage Measurement

The output current from the stimulation sources flows through the safety capacitor and into or out of the tissue. The capacitor gets charged during the sourcing phase and then discharged during the sinking phase. If the current amplitudes in both phases are equal then the voltage at V_{out} in Figure 28 after the stimulation process will perfectly match the voltage prior to the stimulation. Any difference in voltage at the output is indicative of a current mismatch between the sources. Moreover, an increase in this voltage indicates a higher sourcing amplitude whereas a decrease in the voltage after the stimulation implies that the sinking current was higher.

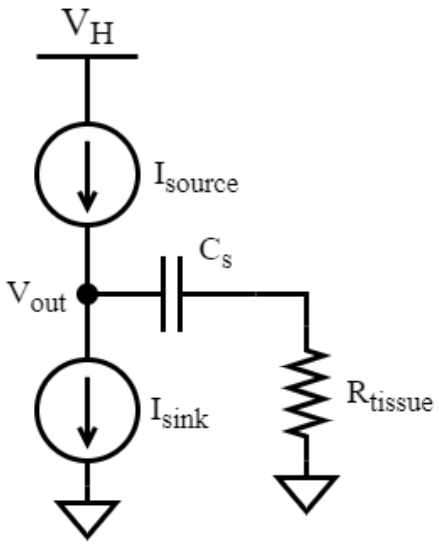

Figure 28: Simplified circuit modelling the current sources, safety capacitor and tissue resistance.

The measurement process has to be done efficiently in terms of current consumption and without affecting the stimulation current. The design proposed measures the voltage changes at the output of the current source that occur due to the stimulation process.

To explore the relationship between the output voltage and current difference further, the waveform for V_{out} is examined in Figure 29. Here, the initial voltage at V_{out} is $V_0 = V_{i1}$, $V_{f1} = V_{i2}$ is the voltage following the sourcing phase and prior to the sinking phase and $V_f = V_{f2}$ is the final voltage after the stimulation process. T/2 is the duration of each stimulation pulse, I_{source} is the sourcing current, I_{sink}

is the sinking current and ΔV_C and ΔV_R are the voltage drops across the safety capacitor C_s and the tissue resistance R, respectively.

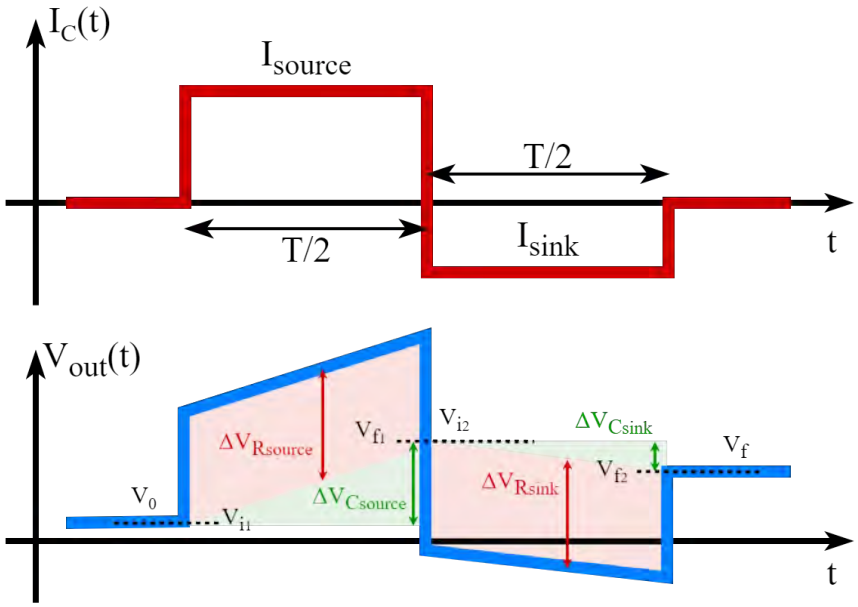

Figure 29: Waveforms representing the stimulation current (current through the safety capacitor) and the output voltage.

The voltage V_{f1} in Figure 29 is given by Equation 2.

$$V_{f1} = \frac{1}{C_s}\left(I_{source}\frac{T}{2}\right) + V_{i1} \tag{2}$$

Similarly, the output voltage after the stimulation pulse is shown in Equation 3. It should be noted that both ΔV_R shift the output voltage upwards and downwards equally without affecting V_f.

$$V_{f2} = \frac{1}{C_s}\left(I_{sink}\frac{T}{2}\right) + V_{i2} \tag{3}$$

Combining Equation 2 and Equation 3 gives the equation for the output voltage following the stimulation as indicated in Equation 4.

$$V_f = \frac{1}{C_s}\left(I_{sink}\frac{T}{2}\right) + \frac{1}{C_s}\left(I_{source}\frac{T}{2}\right) + V_0 \tag{4}$$

Operating with Equation 4 yields Equation 5.

$$V_f - V_0 = \frac{1}{C_s}\frac{T}{2}\left(I_{sink} + I_{source}\right) \tag{5}$$

Given that the sinking current I_{sink} is negative, $I_{sink} + I_{source}$ can be renamed as ΔI representing the current difference between the sources. Equation 6 is obtained by also renaming the voltage difference in Equation 5 as ΔV.

$$\Delta V = \frac{T}{2C_s}\Delta I \tag{6}$$

Equation 6 shows that the difference in the output voltage prior to and following the stimulation pulse (ΔV) is proportional to the difference in the sourcing and sinking currents (ΔI). It can also be seen that ΔV is dependent on the constant values T and C_s but not on the tissue resistance R.

The circuit from Figure 28 was simulated using LTspice XVII by Analog Devices and the resulting waveform for V_{out} is shown in Figure 30. The plot corresponds to a stimulation with a 5 mA sourcing current and three different sinking currents set with a current mismatch of +5%, -1% and -10% (the positive and negative signs indicate whether the sourcing current was higher or lower than the sinking current, respectively). The tissue resistance used in the simulation is 400 Ω, the safety capacitor C_s is 1 µF and the duration of the stimulation pulse is 200 µs.

Figure 30 shows, as expected, that the voltage following the stimulation pulses is different in all three cases. For the +5%, -1% and -10% current mismatch, the simulated ΔV is 25.0 mV, −5.0 mV and −50.0 mV, respectively. These results can also be obtained using Equation 6.

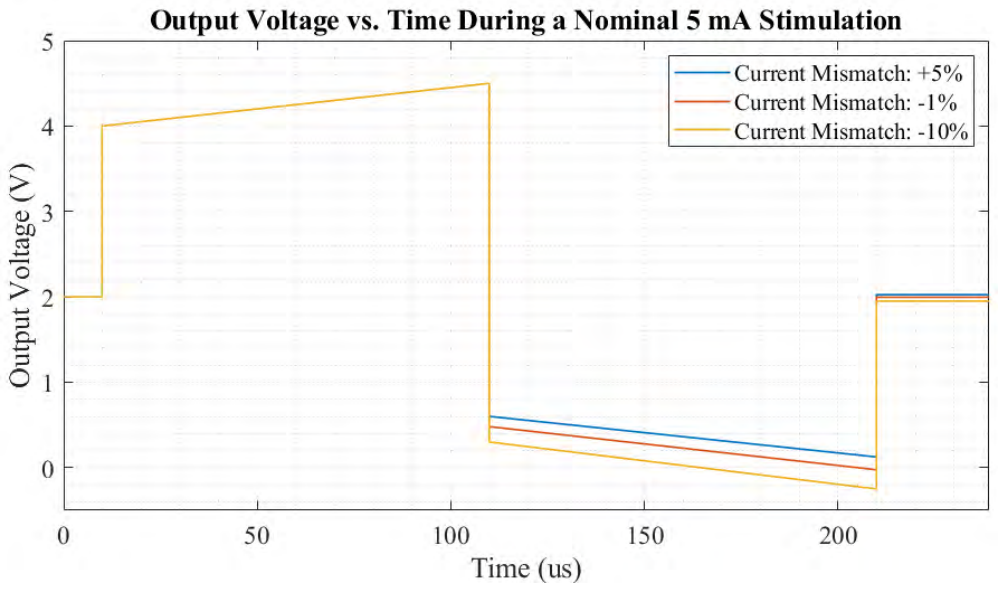

Figure 30: Plot of the output voltage in Figure 28 against time. The sourcing current is 5 mA and the sinking current is set so that the current mismatch is +5%, -1% and -10%.

3.3 Operation Requirements

As indicated in section 3.2, the current mismatch will be measured as the voltage difference at the output of the current source.

Considering a safety capacitor of 1 µF and a calibration pulse of 200 µs, the module should be capable of detecting a ΔV of 100 times the ΔI (Equation 6).

Ideally, the calibration module should be capable of detecting a current mismatch of over 1% or 10 µA. The main priority for the calibration is to precisely measure the mismatch for the higher current levels since it translates into a higher charge imbalance. The 1% value is roughly the minimum difference that the trimming mechanism can fix. This value was set in the design following the indication that a 1% error in a biphasic pulse is considered safe for the stimulation [6]. Using Equation 6, the minimum ΔV that the calibration module is required to detect is 1 mV.

An upper bound will also be determined for testing purposes. As seen in subsubsection 2.2.2.2, most current outputs differ by 5% of the ideal current at the nominal trimming value. This is true in particular for the higher currents which are of interest for setting this upper bound. To keep a safety margin, a maximum of a 10% difference will be used for testing in the designing stage. For the highest output current, this means a current difference of 2.55 mA or a voltage difference of 255 mV.

Therefore, the range for the voltage difference at the input (ΔV) is 1 mV to 255 mV. The requirements from Table 7 are updated in Table 8.

Parameter	**Target Range**
Output	Analog LV output related to the current difference
Input	Analog input in the 0-5 V range
Area	$<$0.345 mm^2
Timing	200 µs calibration pulse
Safety Capacitor	1 µF

Table 8: Operation requirements for the calibration module.

The Computer-Aided Design (CAD) tool used to design the calibration module is Siemens EDA - Mentor Graphics' Pyxis version 20.1 [24].

The project was sent to manufacture and the design was implemented using the technology available which was XFAB's XT018. Unlike XH018, XT018 does not include transistors with a HV gate-source voltage which would be necessary for this implementation. The requirement for the input voltage to remain in the 0 to 5 V range was set considering this limitation and only for academic and research purposes. The circuit, however, should be able to be easily adapted for higher voltages in the 0 to 15 V range.

3.4 Considered Designs

The designs that were considered for the calibration module are presented in this section.

The first circuit that was proposed is shown in the diagram of Figure 31. Unlike the following design where the voltage measuring scheme discussed in section 3.2 (Output Voltage Measurement) is implemented, this design would obtain the current mismatch by measuring the voltage drop across a resistor. It consists of a small measuring resistor R_m, a differential amplifier A and an ADC inside the CPU.

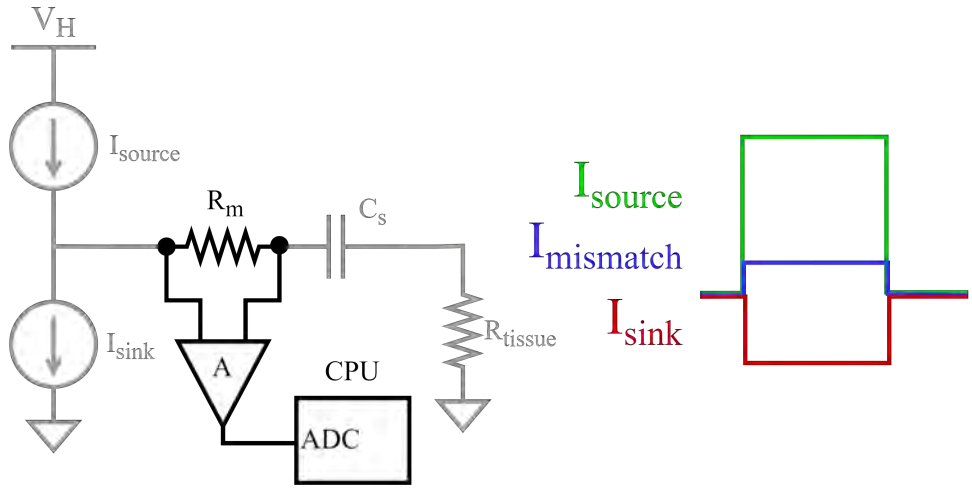

Figure 31: Diagram highlighting the first design proposed for the calibration module. Here, the current mismatch is detected by measuring the voltage drop across the small resistor R_m. To the right is the calibration pulse which is the result of activating both, sourcing and sinking phases simultaneously.

The calibration pulse required for this circuit differs from the biphasic stimulation pulse in that it is generated by activating both internal sources simultaneously as shown in Figure 31. Therefore, the current flowing through R_m is already the resulting mismatch current between the sourcing and sinking phases. The output of the amplifier is thus a scaled version of the current mismatch. This analog voltage is then converted to a digital signal in the ADC and processed by the CPU following the calibration sequence described in section 3.1 (Introduction and Initial Requirements).

As an example, using a $4\,\Omega$ R_m resistor would produce a voltage drop between $400\,\mu V$ and $102\,mV$ for the whole range of output currents. In this case a low offset amplifier would be required. Additionally, since the current source's output may be HV, a future version of the module would have to include a HV low-offset amplifier. Another disadvantage, besides the need for a different type of current pulse, is that the resistor will produce an additional, albeit low, power dissipation with every stimulation.

A second design was proposed considering that the circuit may be adapted to measure the ETI impedance in a future project. This is later discussed in section 6.3.3 (Module for Impedance Measurement).

This second design is presented in Figure 32. Here, a single input is connected to a pair of sample and hold circuits. One of these circuits samples the voltage prior to the stimulation pulse and the second takes a sample following the stimulation. Therefore, the amplifier will output to the ADC a scaled version of the voltage difference ΔV that is proportional to the current mismatch ΔI as shown in section 3.2 (Output Voltage Measurement).

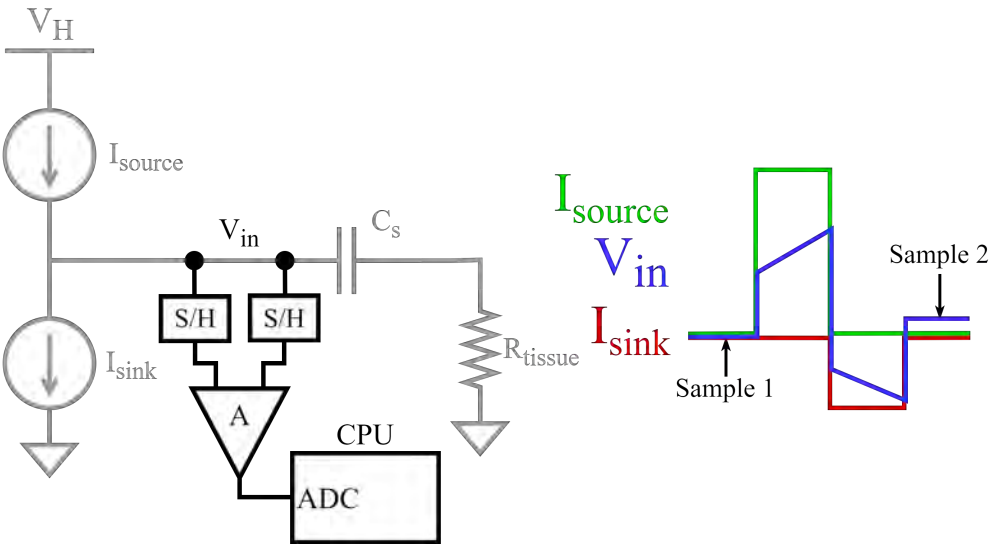

Figure 32: Diagram highlighting the second design proposed for the calibration module. The current mismatch is detected by measuring the output voltage at two different instants. To the right is the calibration pulse showing the instants where the sample and hold circuits sample the input voltage.

Different topologies to implement the sample and hold and amplifier scheme were explored and a Switched-Capacitor (SC) amplifier is proposed. These discrete-time circuits are controlled by switches and operate by transferring charge in and out of capacitors.

SC circuits allow to achieve high efficiencies while requiring less area than the resistor equivalent. With good capacitor matching they can also provide high gain accuracy. SC circuits are usually implemented with offset compensation (Correlated Double Sampling (CDS) technique) to achieve low offset voltages [25].

Figure 33 shows a SC amplifier that is proposed in Reference [26]. The design presented is a differential-to-single-ended amplifier which was adapted in this case to sample the same input signal (V_{in}) at two different instants.

The input sampling phase is activated with pulse ϕ_1. Here, the switches controlled by ϕ_{1IN} and ϕ_{2IN} sample the input on C_1 and C'_1 before and after the calibration pulse, respectively. When the output evaluation phase, ϕ_2, is activated, the charge

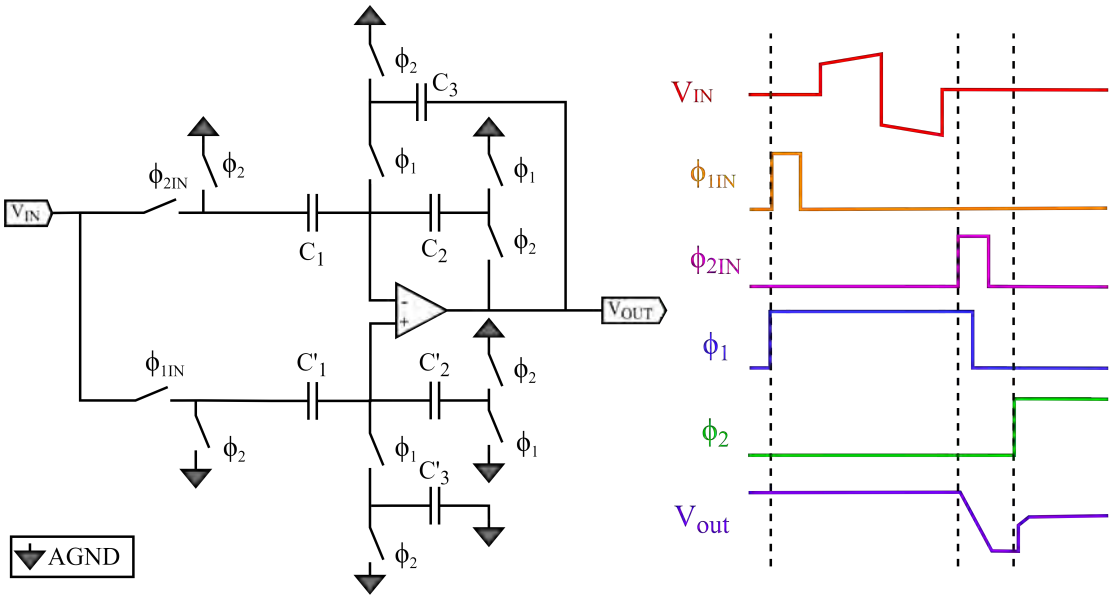

Figure 33: SC amplifier (from Reference [26]). The input, output and switching pulses are shown to the right.

is transferred from C_1 to C_2 and from C'$_1$ to C'$_2$. The gain for this circuit under ideal conditions, i.e. without capacitor mismatch and offset voltage, is $\frac{C1}{C2}$ [25]. Capacitors C_3 and C'$_3$ close the feedback loop during ϕ_1 but assuming no input current to the amplifier, they are not involved in the charge transfer during the phase transitions nor do they affect the circuit's gain.

To test this SC amplifier, the circuit was implemented with a gain of 2 V/v and using an ideal operational amplifier and ideal switches and capacitors. The simulations validated the design for inputs up to 10 V, past this voltage the output would saturate.

One important disadvantage of this implementation is that, as with the previous design, for a HV input, the operational amplifier would have to be a HV low-offset amplifier.

An alternative design is proposed in Figure 34. This SC amplifier works under the same principle than the circuit of Figure 33 but has the advantage of operating with a LV amplifier, requiring less capacitors and switches and using simpler control pulses.

Figure 35 shows the different operating phases for the SC amplifier of Figure 34. During the first phase ϕ_{1a} (Figure 35a), the input voltage prior to the calibration pulse is sampled on capacitor C_{1a}. Similarly, during phase ϕ_{1b} (Figure 35b), the input voltage following the calibration pulse is sampled on C_{1b}.

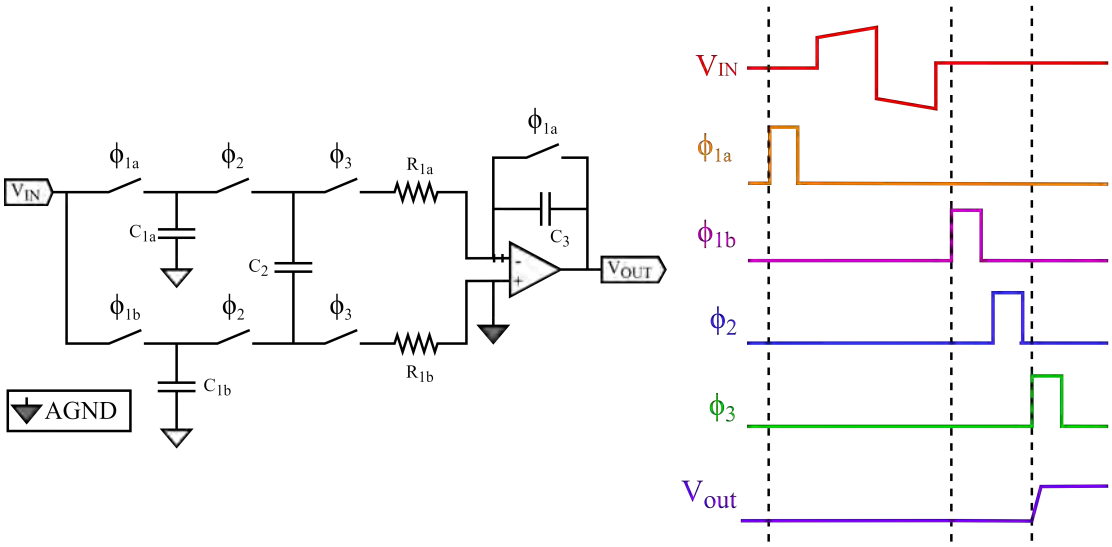

Figure 34: SC amplifier design for the calibration module. The input, output and switching pulses are shown to the right.

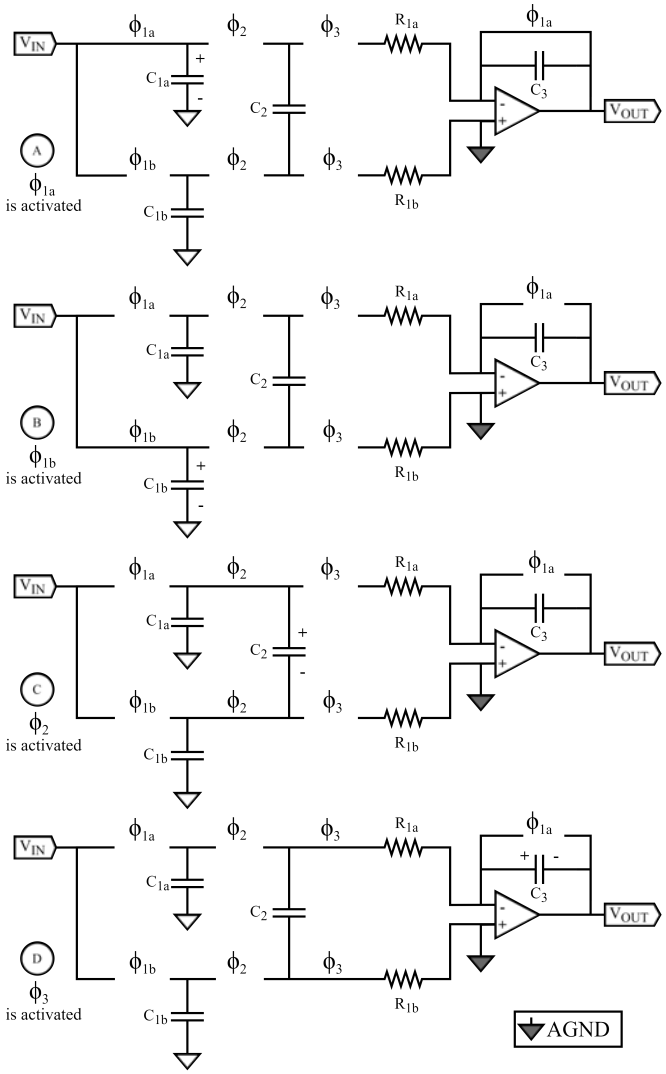

Figure 35: Resulting circuits for all four phases of the SC amplifier design illustrated in Figure 34.

Phase ϕ_2 (Figure 35c) connects capacitors C_{1a} and C_{1b} to the floating capacitor C_2. Therefore, C_2 gets charged with the difference in voltages sampled on C_{1a} and C_{1b}. Then, during phase ϕ_3 (Figure 35d), charge is transferred from C_2 to the feedback capacitor C_3 and the valid output is generated. The positive input of the amplifier is connected to AGND to shift the output voltage.

The advantages mentioned above make this design more suitable for the project.

The following sections deal with the implementation of this SC amplifier.

3.5 Computation of the Gain

In this section, the gain for the schematic design of Figure 34 is computed.

During the first sampling phase (Figure 35a), the charge stored in capacitor C_{1a} is given by Equation 7 where $C_{1a} = C_{1b} = C_1$ and V_a is the input voltage prior to the stimulation.

$$Q_{a0} = C_1 V_a \tag{7}$$

Similarly, the charge stored in capacitor C_{1b} during the phase shown in Figure 35b is given by Equation 8 where V_b is the voltage following the stimulation pulse.

$$Q_{b0} = C_1 V_b \tag{8}$$

V_a and V_b were sampled in capacitors C_{1a} and C_{1b}, respectively. Then, during ϕ_2 (Figure 35c), the capacitor C_2 is connected to capacitors C_{1a} and C_{1b}. Applying Kirchhoff's Voltage Law gives Equation 9 where V_{af} and V_{bf} are the resulting voltages after ϕ_2 and V_2 is the voltage across capacitor C_2.

$$V_{af} - V_2 - V_{bf} = 0 \tag{9}$$

A charge ΔQ is transferred from capacitors C_{1a} and C_{1b} to capacitor C_2. Substituting this in Equation 9 gives Equation 10.

$$\frac{Q_{a0} - \Delta Q}{C_1} - \frac{\Delta Q}{C_2} - \frac{Q_{b0} + \Delta Q}{C_1} = 0 \tag{10}$$

Simplifying Equation 10 yields Equation 11.

$$\frac{Q_{a0} - Q_{b0}}{C_1} - \left(\frac{2\Delta Q}{C_1} - \frac{\Delta Q}{C_2}\right) = 0 \tag{11}$$

Combining Equation 11 with Equation 7 and Equation 8 gives Equation 12.

$$(V_a - V_b) = \Delta Q \left(\frac{2C_2 + C_1}{C_1 C_2} \right) \tag{12}$$

Solving for ΔQ gives Equation 13.

$$\Delta Q = (V_a - V_b) \frac{C_1 C_2}{2C_2 + C_1} \tag{13}$$

During phase ϕ_3 (Figure 35d) the final charge stored in capacitor C_3 (Q_{3f}) is given by Equation 14 where V_{os} is the offset of the operational amplifier.

$$Q_{3f} = \Delta Q - V_{os} C_2 \tag{14}$$

Applying Kirchhoff's Voltage Law to find the output voltage V_{out} results in Equation 15.

$$V_{out} = \frac{\Delta Q - V_{os} C_2}{C_3} - V_{os} \tag{15}$$

Substituting ΔQ in Equation 15 yields Equation 16.

$$V_{out} = -(V_b - V_a) \frac{C_1 C_2}{C_3 (2C_2 + C_1)} - V_{os} \left(1 + \frac{C_2}{C_3} \right) \tag{16}$$

Therefore, taking $V_{in} = (V_b - V_a)$ and considering that the offset voltage will be minimized, the gain G of the circuit is given by Equation 17.

$$G = -\frac{C_1 C_2}{C_3 (2C_2 + C_1)} \tag{17}$$

3.6 Global Operation

3.6.1 Simulation of the Ideal Circuit

The circuit shown in Figure 34 was simulated in Mentor Graphics' Pyxis using ideal components (switches, operational amplifier and capacitors). The simulations presented in the following sections were performed for a temperature of 37 °C since this is representative of the temperature of the human body[1].

The switching capacitors were selected considering the gain and area constraints. Any absolute gain greater than unity makes the circuit directly compatible with the 12-bit ADC that will be connected to the output.

[1]Some simulations were also performed in the 35 °C to 45 °C range observing no significant change in the output voltage with a maximum variation of 0.07%.

The capacitance values for the design were picked after several iterations and the results are presented in Table 9. With these values, the input voltages can be correctly sampled and held. Equation 17 shows that the circuit achieves a gain of -2.4 $^{V}/_{V}$.

Capacitor	**Value**
C_{1a}	40 pF
C_{1b}	40 pF
C_2	30 pF
C_3	5 pF

Table 9: Capacitor values selected for the design of the SC amplifier.

Table 10 shows the results of the simulation. Eight sets of ΔV inputs were generated for the calibration module to measure. The module's output is related to the ΔV as shown in Equation 18. Both the input and measured ΔV from the simulation are compared and the error is computed.

$$\Delta V_{measured} = \frac{V_{out} - V_{AGND}}{G} \tag{18}$$

As shown in Table 10, the resulting errors for inputs greater than 10 mV are less than 1%. The error for 1 mV, which is the lowest ΔV input, is slightly higher.

The results obtained in this first simulation are adequate to validate the preliminary design. In the following subsections, the SC amplifier is implemented with real models for the components and the simulation is repeated.

3.6.2 Capacitor Selection

The values for the capacitors are shown in Table 9 and were simulated to verify that they are capable of correctly sampling and holding the input voltages. As discussed in section 3.6.1 (Simulation of the Ideal Circuit), the gain of the circuit is determined by Equation 17 and is thus -2.4 $^{V}/_{V}$.

The model selected for the capacitors is the csf4a from XFAB's XT018 Primitive Library. The minimum and maximum applied voltage for this model is -60 V and 60 V, respectively. Using HV capacitors in this design allows to easily migrate to a future HV implementation of the calibration module.

The csf4a capacitors are implemented using metals one through four which gives them a greater area capacitance (0.51 $\frac{\text{fF}}{\mu\text{m}^2}$). Considering this parameter and the values selected for the capacitors, a total area of 0.225 mm^2 is estimated for these devices (without dummy capacitors).

ΔV input (mV)	Measured output (V)	ΔV measured (mV)	Error
1	1.652	0.9	-6%
-1	1.647	-1.1	6%
10	1.674	9.9	-1%
-10	1.626	-10.1	1%
100	1.890	100.0	0%
-100	1.410	-100.0	0%
255	2.262	255.0	0%
-255	1.039	-255.0	0%

Table 10: Simulation results for the SC amplifier using ideal components. ΔV is the difference in the input voltage prior to and following the stimulation pulse. The measured output is the simulated output of the calibration module. ΔV measured is computed from the output of the module according to Equation 18. The error between this magnitude and the actual ΔV input is shown in the last column.

3.6.3 Design of the Switches

Transmission Gates (TGs) are used as the switching elements in Figure 34. These devices are implemented as two Complementary Metal-Oxide-Semiconductor (CMOS) transistors connected back-to-back in parallel as shown in Figure 36. The inverter is used to generate the two complementary control voltages for the NMOS and PMOS transistors. The TG is therefore a symmetric device which makes the input and output interchangeable. The device can perform correctly as a switch while the current flows in both directions.

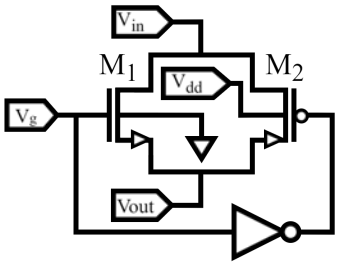

Figure 36: Implementation of the switches using transmission gates.

The transistors used were the standard 5 V NMOS and PMOS transistors, ne5 and pe5, respectively from XFAB's XT018 Primitive Library. They can withstand V_{gs} and V_{ds} voltages from $-5.5\,V$ to $5.5\,V$.

The transistors were selected to have the smallest size possible to reduce charge injection at the expense of a higher ON resistance (r_{on}). The width (W) and length (L) of both transistors are shown in Table 11. The same TG was used for all switches.

Transistor	Width (µm)	Length (µm)	Multiplier
M1	0.5	0.5	1
M2	0.5	0.5	1

Table 11: Transistor sizes for the TG of Figure 36.

Figure 37 shows the plot of the ON resistance against the output voltage when the TG is enabled. It can be seen that the maximum r_{on} for the TG is 20 kΩ.

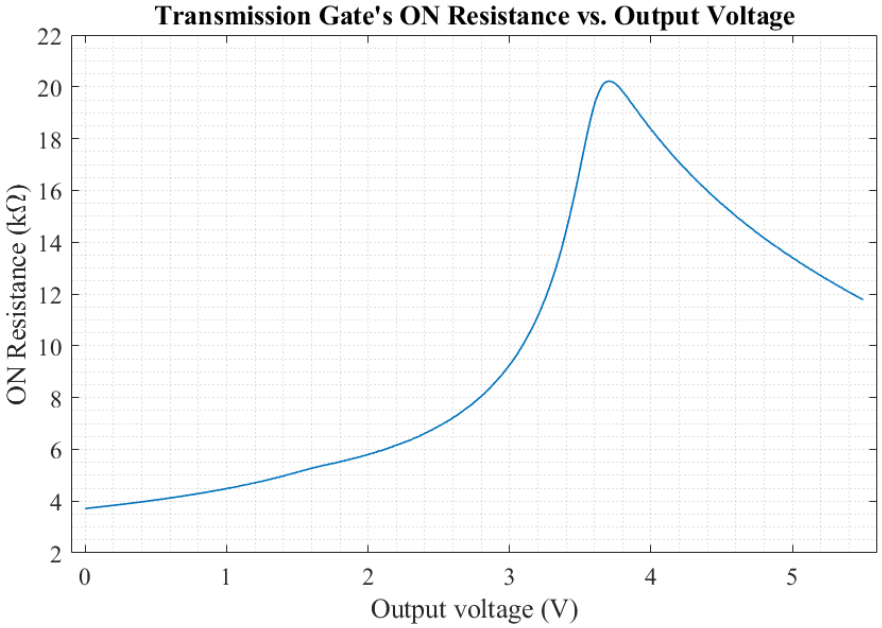

Figure 37: Plot of the TG's ON resistance against the output voltage when the device is enabled.

In order to verify that this maximum r_{on} does not affect the correct operation of the module, the worst-case for the time constant τ is analyzed. The largest capacitance connected to a switch when it is activated is of 40 pF. Therefore, the maximum τ can be computed as shown in Equation 19.

$$\tau_{max} = R_{ONmax} \cdot C_{max} = 20k\Omega \cdot 40\rho F = 800ns \tag{19}$$

The resulting value for the maximum τ is much lower than the time the switch will be activated so the operation of the module should not be affected. To test this further, the simulation from section 3.6.1 (Simulation of the Ideal Circuit) was repeated using ideal switches with an ON resistance of 20 kΩ. The results from Table 10 remain unchanged.

The simulation is repeated once again. This time replacing all switches with the TGs implemented. The results are shown in Table 12.

Ideal input (mV)	Measured output (V)	Measured input (mV)	Error
1	1.652	0.8	-17%
-1	1.647	-1.2	17%
10	1.674	9.8	-2%
-10	1.626	-10.2	2%
100	1.889	99.7	0%
-100	1.410	-100.0	0%
255	2.261	255.0	0%
-255	1.037	-255.0	0%

Table 12: Updated simulation results for the SC amplifier using the TGs implemented, an ideal operational amplifier and ideal capacitors.

The module continues to exhibit a correct behavior for the higher ΔV inputs. For the lower ΔV inputs, the error is increased and it is observed that a constant offset voltage is added to the output. This is believed to be caused by charge injection introduced by the transmission gates. Dummy transistors were included to reduce this effect, but to no avail. To correct this issue, a CDS compensation system is implemented as described in section 3.6.4 (Correlated Double Sampling). This technique is widely adopted to suppress the effects of DC offset in sampled-data systems, particularly in SC circuits [27] [28].

3.6.4 Correlated Double Sampling

The CDS technique allows to cancel an undesired DC offset by sampling the output signal twice and computing the difference between these correlated samples. Generally, the output is first measured under a known condition and then measured again under an unknown condition [29].

In this case, to eliminate the undesired DC offset in the output signal, the CDS correction will be applied as shown in Figure 38. The calibration module will perform an additional sampling step (referred to as the "CDS run") whereby the input voltage is sampled without any current stimulation. Therefore, both of the samples taken by the module during the CDS run should be roughly the same (i.e. the input ΔV is 0 V- this is akin to short-circuiting the inputs to measure the offset but at different instants). The output of the calibration module (V_{CDS}) is then stored in the chip's memory.

Once the CDS run is completed, the calibration routine is performed regularly and the measured ΔV can be computed from the module's output using V_{CDS} as shown in Equation 20, which replaces Equation 18.

$$\Delta V_{measured} = \frac{V_{out} - V_{CDS}}{G} \tag{20}$$

The resulting ΔI is then computed according to Equation 6.

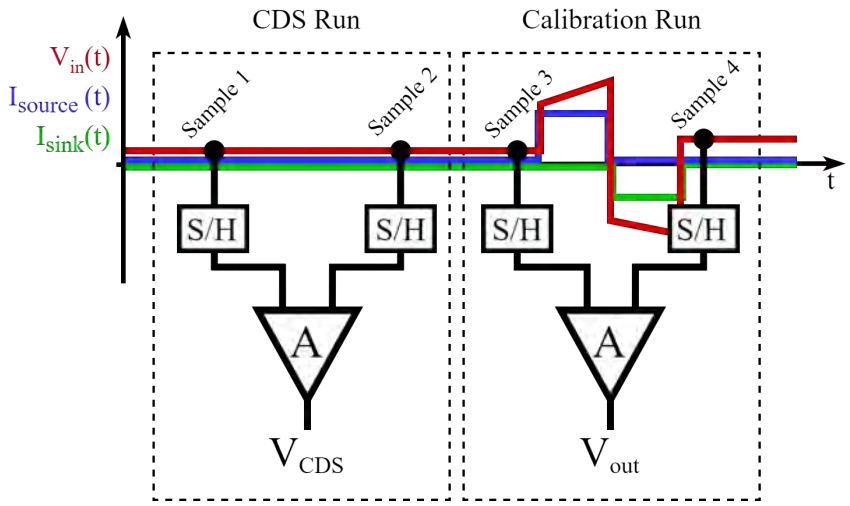

Figure 38: Operation of the calibration module using the CDS technique. The input voltage, sinking and sourcing currents are plotted against time. The illustration shows the module performing the same routine for the calibration and CDS runs, with and without the presence of a stimulation pulse.

Figure 39 shows the updated sequence of steps to be followed by the module in order to perform the complete calibration routine. The additional CDS run is executed only once at the beginning.

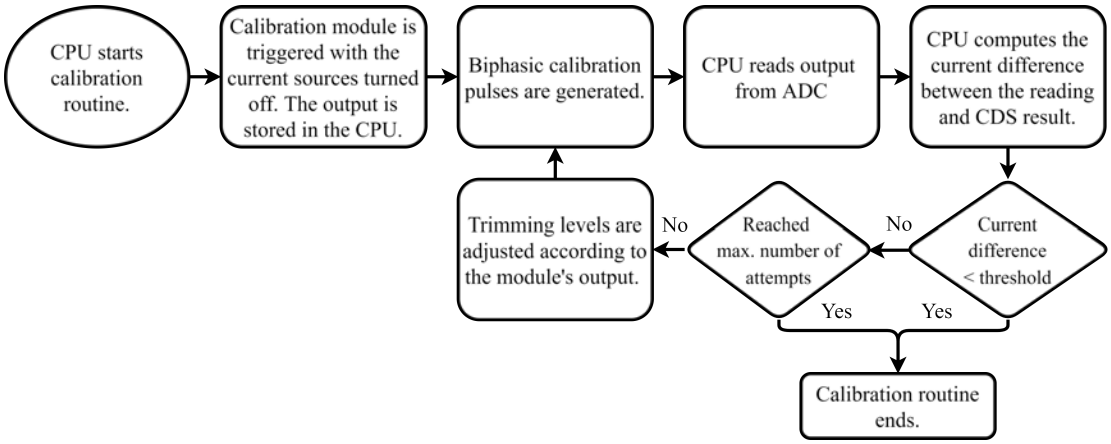

Figure 39: Updated flowchart showing the sequence of steps for the calibration routine using the CDS technique.

To validate the application of this technique, the simulation from section 3.6.3 (Design of the Switches) is repeated with the same TGs, ideal capacitors and an ideal operational amplifier except this time the CDS correction is applied. The results are shown in Table 13. It can be seen that all errors fall below 1% and most importantly, the errors for the highest nominal currents are negligible.

ΔV input (mV)	Measured output (V)	ΔV measured (mV)	Error
0	1.650	-	-
1	1.652	1.0	1%
-1	1.647	-1.0	-1%
10	1.674	10.0	0%
-10	1.626	-10.0	0%
100	1.889	99.9	0%
-100	1.410	-100.0	0%
255	2.261	255.0	0%
-255	1.037	-255.0	0%

Table 13: Updated simulation results for the SC amplifier using the TGs implemented, an ideal operational amplifier and ideal capacitors and applying the CDS compensation technique. The first row corresponds to the CDS run.

3.6.5 Digital Design

In order to command the switches, the control pulses shown in Figure 34 need to be generated (i.e. ϕ_{1a}, ϕ_{1b}, ϕ_2 and ϕ_3). These four individual pulses are spaced with delays on the order of tens to hundreds of µs.

Instead of requiring a separate input for each pulse, only one signal containing all four pulses (Clk) will be the input to the module. This is illustrated in Figure 40. To initialize the sequence, the Clk signal also contains a short reset pulse and there is an additional enable input.

The outputs y_0, y_1, y_2 and y_3 shown in Figure 40 are the ϕ_{1a}, ϕ_{1b}, ϕ_2 and ϕ_3 signals from Figure 34, respectively.

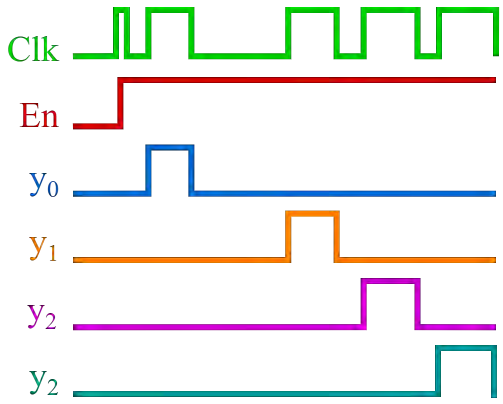

Figure 40: Input (Clk and En) and output (y_0, y_1, y_2 and y_3) signals to control the activation of the switches.

The Finite-State Machine (FSM) in Figure 41 is implemented to extract the four individual pulses from the Clk signal to control the gates of the TGs. The output for each state is shown in Table 14.

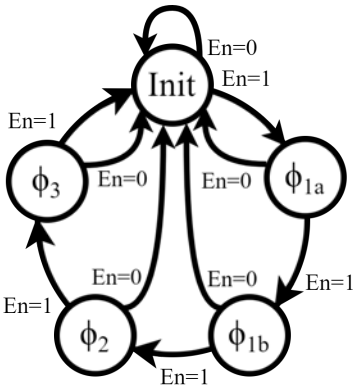

Figure 41: FSM design for the switching signals.

State	Outputs			
	$\mathbf{y}_0$	$\mathbf{y}_1$	$\mathbf{y}_2$	$\mathbf{y}_3$
Init	0	0	0	0
ϕ_{1a}	1	0	0	0
ϕ_{1b}	0	1	0	0
ϕ_2	0	0	1	0
ϕ_3	0	0	0	1

Table 14: Outputs (y_0, y_1, y_2 and y_3) for each state of the FSM.

The digital circuit is implemented with three state variables (Q0, Q1 and Q2) and hence three D flip-flops. Using the characteristic equation of the D flip-flop ($Q^* = D$) and solving the Karnaugh maps for the FSM yields Equation 21.

$$\begin{cases} D_0 = Q_1' \cdot En \\ D_1 = Q_0 \cdot En + Q_2' \cdot Q_1 \cdot En \\ D_2 = Q_2' \cdot Q_1 \cdot Q_0' \cdot En \end{cases} \tag{21}$$

The outputs y_0 through y_3 are given by Equation 22.

$$\begin{cases} y_0 = Clk \cdot Q_2' \cdot Q_1' \cdot Q_0 \\ y_1 = Clk \cdot Q_2' \cdot Q_1 \cdot Q_0 \\ y_2 = Clk \cdot Q_2' \cdot Q_1 \cdot Q_0' \\ y_3 = Clk \cdot Q_2 \cdot Q_1 \cdot Q_0' \end{cases} \tag{22}$$

The circuit designed from Equation 21 and Equation 22 is shown in Figure 42.

Standard library logic gates provided in XT018 (D_CELLS_5V library) were used for the implementation. The DFRRQ_5VX1 is selected as the positive-edge triggered D flip-flop.

The circuit was simulated and validated. The results are plotted in Figure 43.

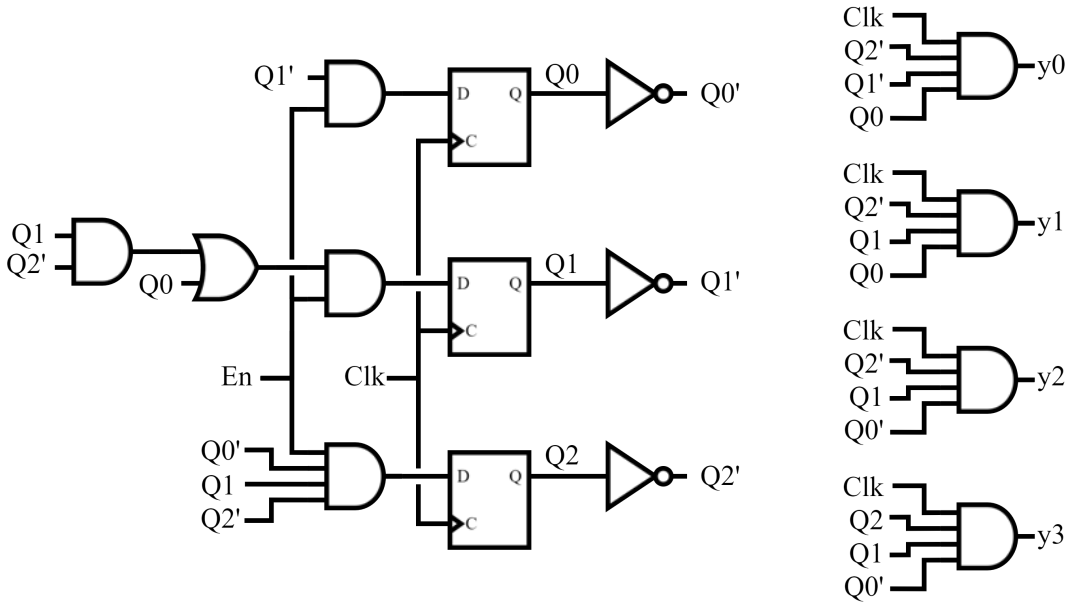

Figure 42: Schematic implementation of the FSM from Figure 41.

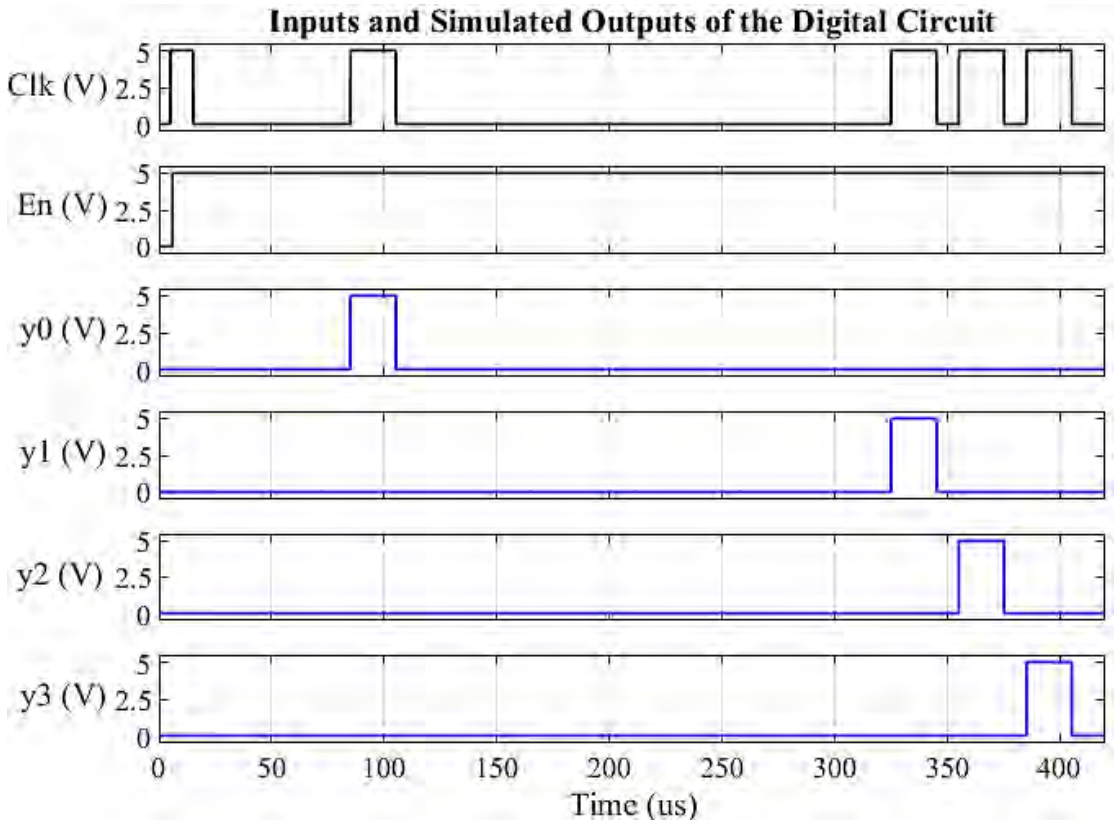

Figure 43: Simulation results for the digital circuit in Figure 42. The clock and enable inputs are shown in the top two rows and the bottom plots are the simulated outputs y0 through y3.

3.6.6 Design of the Operational Amplifier

A basic operational amplifier with the following requirements is designed:

- Voltage supply of 5 V.
- Current consumption of less than 3 µA.
- Minimum offset (a systematic offset of 10 µV).
- Total area of a few thousand µm^2.

The operational amplifier is implemented using the standard 5 V transistors, ne5 and pe5. The schematic design[2] is shown in Figure 44.

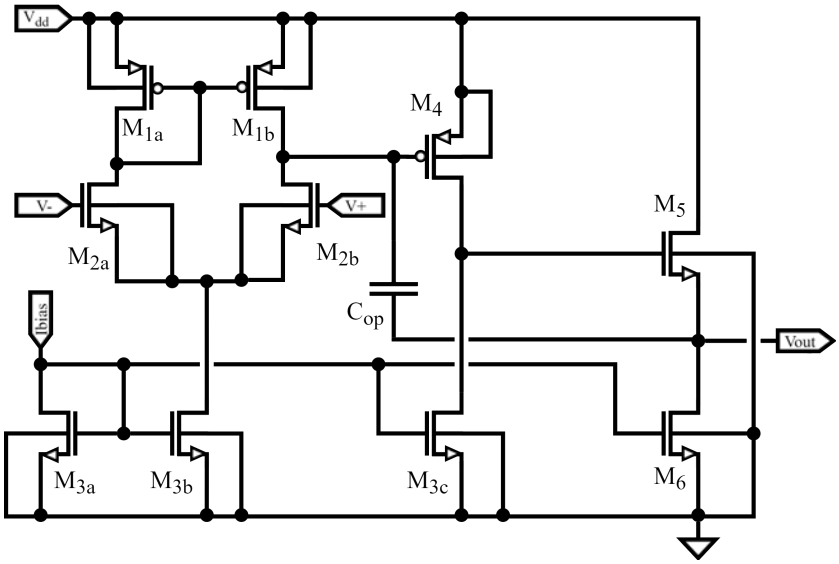

Figure 44: Schematic design of the operational amplifier.

The sizes for the transistors are estimated using the Advanced Compact MOSFET (ACM) model [30]. Equation 23 and Equation 24 show the expressions for the saturation drain-source current (I_D) and the transconductance (g_m). The sizes are later verified with the simulations which are based on the BSim4v5.7 model [31].

$$I_D = i_f \frac{n\mu C'_{ox}\phi_T^2}{2}\frac{W}{L} \tag{23}$$

$$g_m = \frac{2I_D}{n\phi_T(1+\sqrt{1+i_f})} \tag{24}$$

For Equation 23 and Equation 24, ϕ_T is the thermal voltage which is approximately 26 mV. C'_{ox} is the capacitance of the gate's oxide and it is provided by the manufacturer. The parameter n is the slope factor which ranges between one

[2]The circuit was adapted from a comparator designed by Natalia Martínez and Juan Sapriza for the Microelectronics course to fit the requirements of this specific application.

and two and is dependent on the transistor. On the other hand, i_f represents the inversion level. For $i_f \leq 1$, the transistor is said to operate in Weak Inversion (WI). For $i_f \geq 100$, the transistor is in the Strong Inversion (SI) region and for $1 \leq i_f \leq 100$, it is in the Moderate Inversion (MI) region.

The dimensions for the differential pair transistors (M_{2a} and M_{2b}) were selected so that they would operate in the WI region. This can help achieve less offset and a greater gain to power consumption ratio at the expense of requiring more area. For these transistors, an L greater than three times the minimum length is selected to avoid short canal effects [32]. An initial value of 0.1 was chosen for i_f and W was calculated using Equation 23. The values were later adjusted using the simulator. The final dimensions selected for the design are shown in Table 15.

Transistors	**Width (µm)**	**Multiplier**	**Total Width (µm)**	**Length (µm)**
M1	1	5	5	5
M2	5	6	30	0.9
M3	0.5	4	2	2
M4	1	10	10	5
M5	0.5	4	2	2
M6	0.5	4	2	2
Total Area			170 μm^2	

Table 15: Transistor sizes for the operational amplifier.

The transistors M_{1a} and M_{1b} are used to implement a current mirror. They are designed to operate in MI and have a similar area to those of the differential pair. The M_{3a}, M_{3b}, M_{3c} and M_6 transistors are also used for current mirrors and operate in the MI region to improve the precision of the current copy (a 1:1 copy is used).

The amplifier transistor M_4 was designed to have a similar size than the current mirror transistors M_1 and adjusted to minimize the offset. Finally, M_5 is used to implement a common-drain amplifier to buffer the output.

For the compensation capacitor (C_{op} in Figure 44), a 1 pF csf4a capacitor is selected. The frequency response was simulated and it is presented in the Bode plot of Figure 45. It can be seen that the phase margin is 81° and the gain margin is 8 dB which shows that the system is stable [33].

The operational amplifier's systematic offset is estimated by simulating the output voltage while sweeping the differential input voltage. Figure 46 shows the result of the simulation for different transistor models. For the Typical model, an offset of 9 µV is measured. For the Worst Power and Worst Speed transistors, the measured output offsets are 8 µV and 11 µV, respectively. A Monte Carlo simulation was also used to measure the random offset which resulted in a mean value of 60 µV and a standard deviation of 2.36 mV. This standard deviation may be reduced by using larger transistors.

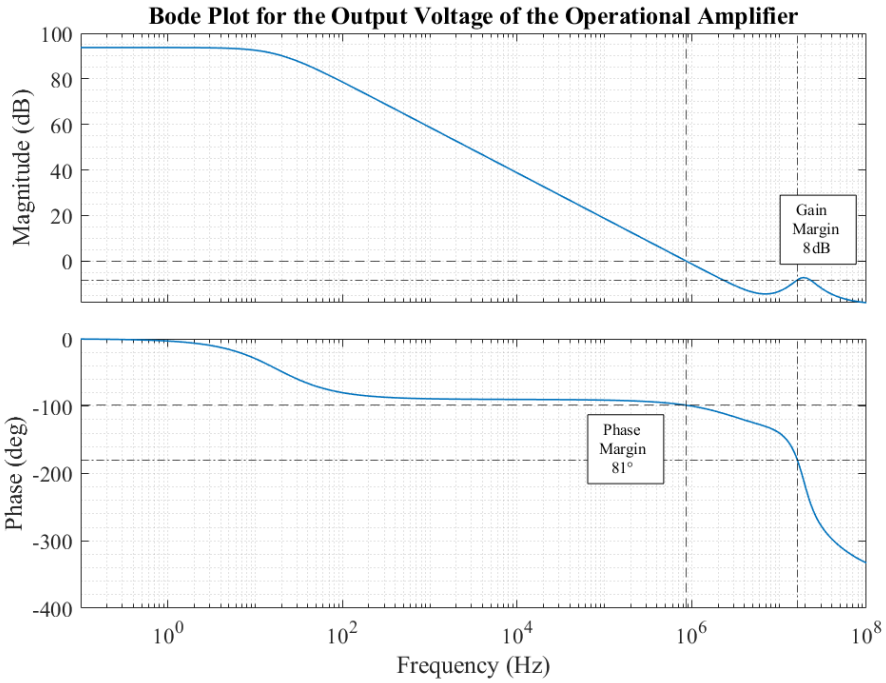

Figure 45: Frequency response for the output of the operational amplifier. The gain and phase margins are indicated.

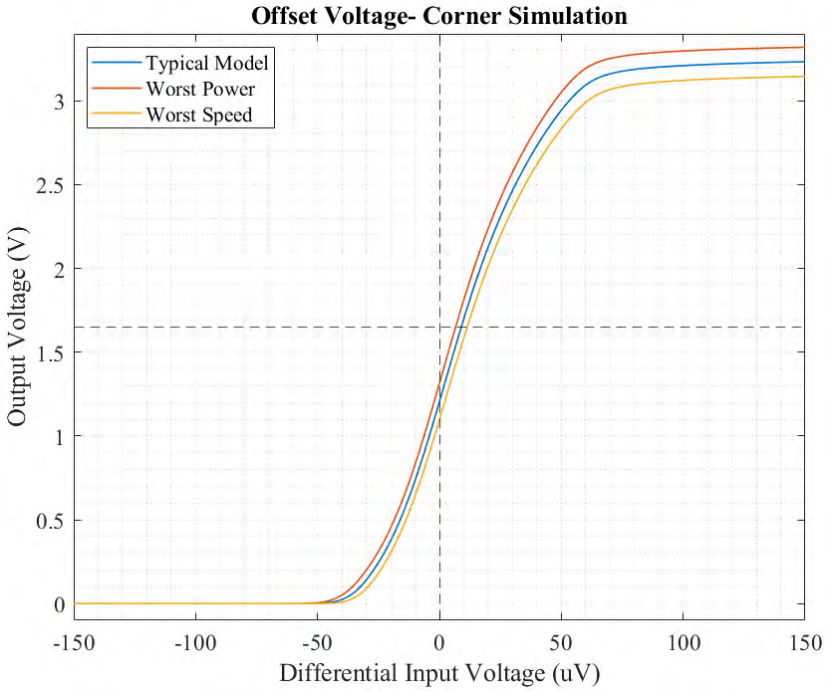

Figure 46: Plot of the output voltage of the operational amplifier against the differential input voltage. The common mode voltage used is $\frac{V_{DD}}{2}$. The simulation was performed for three different transistor models (Typical, Worst Speed and Worst Power).

The simulation is repeated for the Typical model transistors varying the common mode voltage at the input (Figure 47). The measured offset voltages are 23 µV and −5 µV for a common mode input voltage of 1.5 V and 3.5 V, respectively.

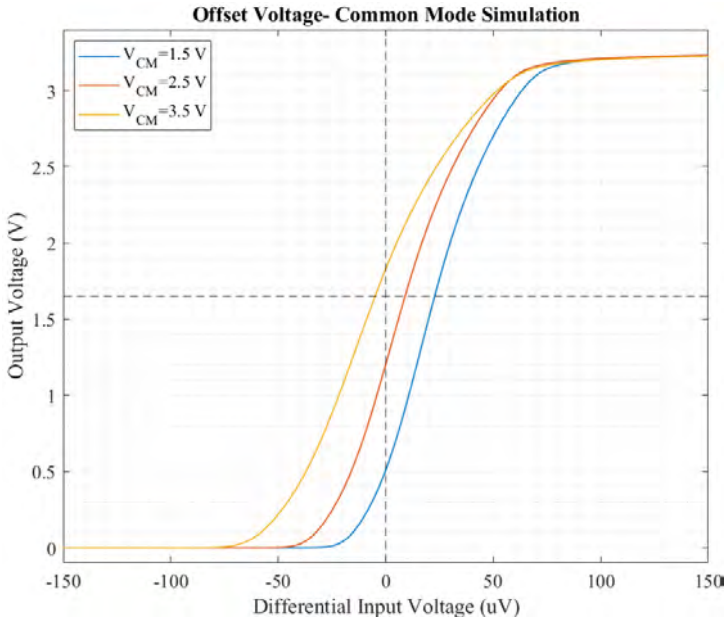

Figure 47: Plot of the output voltage of the operational amplifier against the differential input voltage. The simulation is performed with three different common mode voltages at the inputs (1.5 V, 2.5 V and 3.5 V) using the Typical model for the transistors.

The response time is also characterized in the simulation shown in Figure 48. A voltage step is applied to one of the inputs while the other remains constant. The operational amplifier saturates after a delay of 4.2 µs for the Worst Power model, 4.7 µs for the Typical model and 5.1 µs for the Worst Speed model.

In this application, speed optimization is not a priority. In practice, the response time can be fixed by generating calibration pulses longer than the measured delay.

The parameters measured for the operational amplifier are summarized in Table 16 along with the target values as per the requirements.

Parameter	**Design**	**Target**
Supply Voltage	5 V	5 V
Current consumption	1.5 µA	<3 µA
Systematic offset	9 µV	<10 µV
Area	1400 µm²*	∼1000 µm²
Response time	5 µs	-

Table 16: Simulated parameters for the operational amplifier designed and the corresponding target values. *The layout of the operational amplifier is presented in section 4.2.

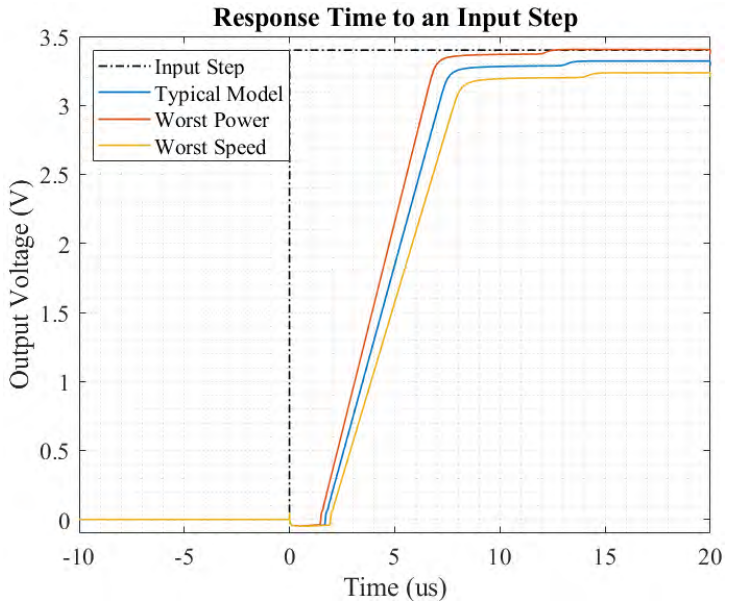

Figure 48: Response time to an input step. The transient simulation was performed for three different transistor models (Typical, Worst Speed and Worst Power).

3.6.7 Final Design

The simulation of the calibration module is repeated with the components designed and using the CDS technique. The results are shown in Figure 49. The simulation was performed using a set of different input ΔV and V_{CM} as indicated in Table 17. From these results the best, average and worst error waveforms are plotted. It can be seen that for the higher input ΔV, the error lies below 1% in all of the cases simulated. For the lower input ΔV the error is more sensitive to the input V_{CM}. This simulation is repeated in section 4.5 (Pads and Buffers) after the implementation of the layout.

An example of the output's waveform is shown in Figure 50. The sourcing and sinking current mismatch was simulated to produce an input ΔV of 100 mV. The plot also indicates the instants where the CDS and the calibration samples are taken as well as the time from which the outputs are valid. The measured ΔV can be computed from the output voltage using Equation 20.

Testing V_{CM} (V)	1.0	1.5	2.0	2.5	3.0	3.5	4.0
Testing ΔV (mV)	$\pm$1	$\pm$10	$\pm$20	$\pm$50	$\pm$80	$\pm$100	$\pm$130
	$\pm$160	$\pm$190	$\pm$220	$\pm$255	$\pm$275	$\pm$300	

Table 17: Set of V_{CM} and ΔV values that form the input combinations used to simulate the output of the calibration module. The input is defined as V_{CM} prior to the stimulation pulse and $V_{CM} + \Delta V$ following the stimulation.

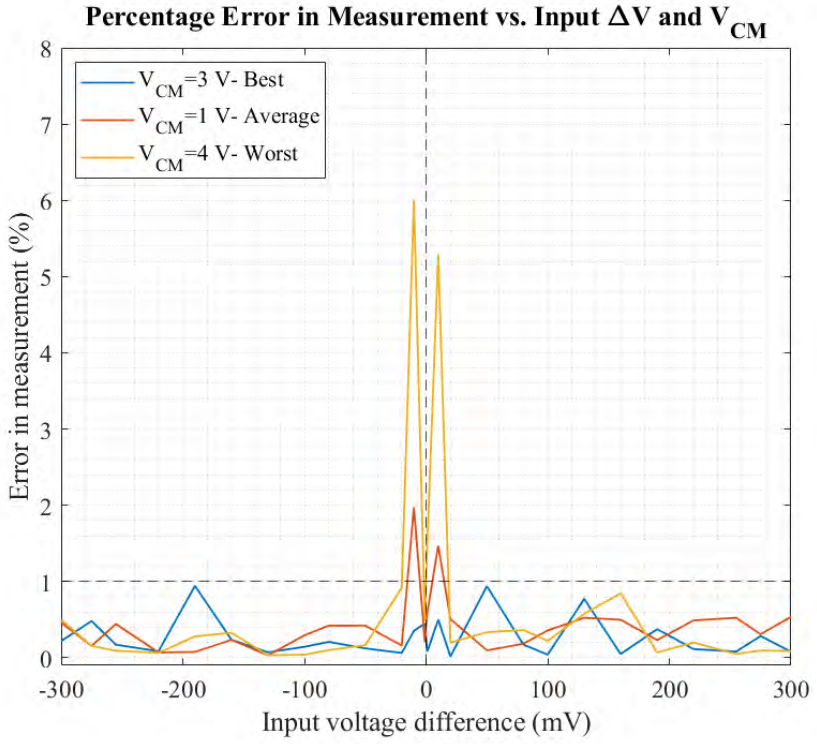

Figure 49: Simulation results of the SC amplifier using the components designed and applying the CDS compensation technique. The input V_{CM} and ΔV used in the simulations are indicated in Table 17. The best, average and worst results from these simulations are presented in the plot.

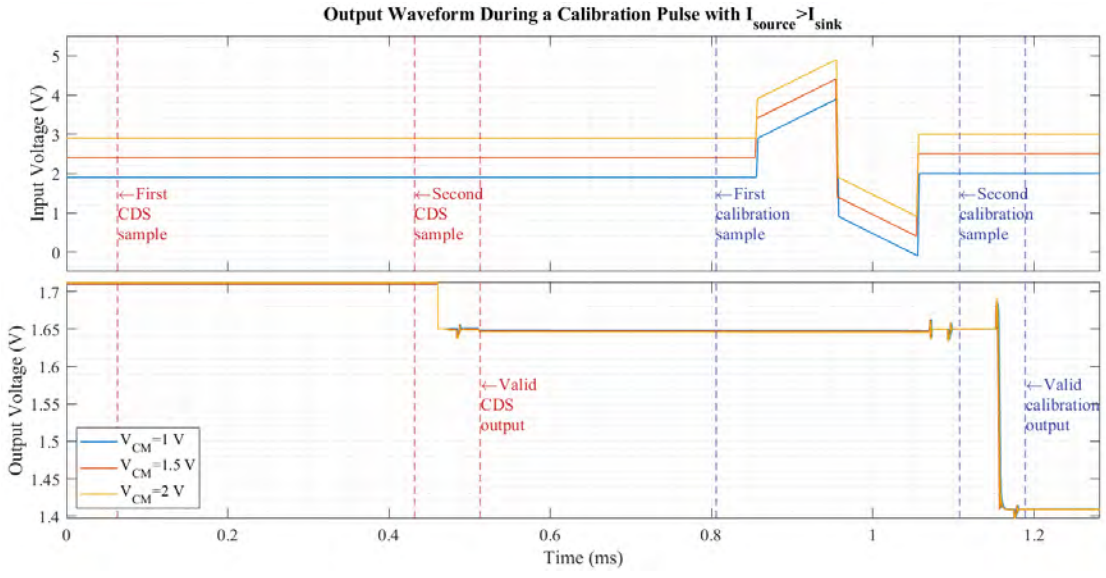

Figure 50: Waveform of the output voltage of the calibration module while performing the CDS and a single calibration run.

3.7 Conclusions

In this section, the schematic for the calibration module was designed and implemented. The module operates according to the diagram of Figure 39. The calibration pulses are 200 µs long and a 1 µF safety capacitor is required for this design.

The LV output of the calibration module is related to the current mismatch. To obtain the percentage current mismatch from the module's output, the CPU needs to perform the operation indicated in Equation 25 which results from combining Equation 20 and Equation 6. Here, $I_{nominal}$ is the stimulation current programmed.

$$\Delta I_{\%} = 100 \cdot \frac{2C_s}{GTI_{nominal}}(V_{out} - V_{CDS}) \tag{25}$$

When $\Delta I_{\%} > 0$, the sourcing current needs to be decreased or the sinking current increased to achieve the balance. Conversely, if $\Delta I_{\%} < 0$, then either the sourcing current needs to be increased or the sinking current decreased. This adjustment is performed by means of the trimming mechanism implemented in the current sources. The percentage difference allows to quantify the trimming levels to be skipped and programmed for the currents to be matched.

Part 4

Layout of the Calibration Module

This section presents the physical design of the calibration module.

The implementation of the design involves placing and routing components and cells using a set of widely-followed layout practices. Matching techniques are used in this design to make capacitor and transistor arrays that prevent the individual devices from being affected differently by effects caused in the manufacturing process. This makes the design more sensitive to differential variability as opposed to absolute variability [34].

4.1 Capacitors

As indicated in section 3.6.2 (Capacitor Selection) the model used for the capacitors is the csf4a which are implemented in unit cells of 32.9 fF.

The capacitors included in the design of the circuit are listed in Table 18. C_{1a}, C_{1b}, C_2 and C_3 total up 115 pF and require careful matching since the performance of the calibration module is sensitive to these values. The 1 pF compensation capacitor of the operational amplifier C_{op} is also included in this layout.

Capacitor	**Value**	**Matching code**
C_{1a}	40 pF	E
C_{1b}	40 pF	D
C_2	30 pF	C
C_3	5 pF	B
C_{op}	1 pF	A
Dummies	32.9 fF - 1pF	F

Table 18: Capacitors used in the design. The matching code is the identification used to implement the layout array.

Individual capacitors of 1 pF were implemented using 32 units of the cells provided and were placed in an array of 13 rows and 9 columns.

Each capacitor is positioned to achieve a common centroid [35]. This arrangement allows to distribute the capacitors so that any effect that may alter the capacitance affects all devices equally, eliminating linear variations due to first-order process gradients [34]. The array designed is shown in Figure 51.

Additional capacitors known as "dummy" devices are short-circuited to ground and placed in the array to protect the circuit from edge effect imperfections that may arise in the manufacturing process. Most dummy capacitors are made smaller than the 1 pF cell to optimize space but large enough to surround the outermost capacitors.

Figure 52 shows the final layout with all capacitors from Table 18. The csf4a are implemented using metals one through four and were routed with the fifth and sixth metal layers. This was done using metal wires of dimensions that are able

F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
F	C	D	D	E	D	D	C	D	D	E	D	D	C	F
F	E	E	C	E	C	E	C	E	C	E	C	E	E	F
F	D	E	D	C	D	E	B	E	D	C	D	E	D	F
F	E	D	E	D	E	D	B	D	E	D	E	D	E	F
F	C	C	B	C	C	C	A	C	C	C	B	C	C	F
F	E	D	E	D	E	D	F	D	E	D	E	D	E	F
F	D	E	D	C	D	E	C	E	D	C	D	E	D	F
F	E	E	C	E	C	E	B	E	C	E	C	E	E	F
F	C	D	D	E	D	D	C	D	D	E	D	D	C	F
F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

Figure 51: Capacitor array implemented. The references are found in Table 18.

to withstand the supplied currents and exhibit a low resistance. Via redundancy is also used in the connections.

This block has a total capacitance of 126 pF and a total area of 0.291 mm^2.

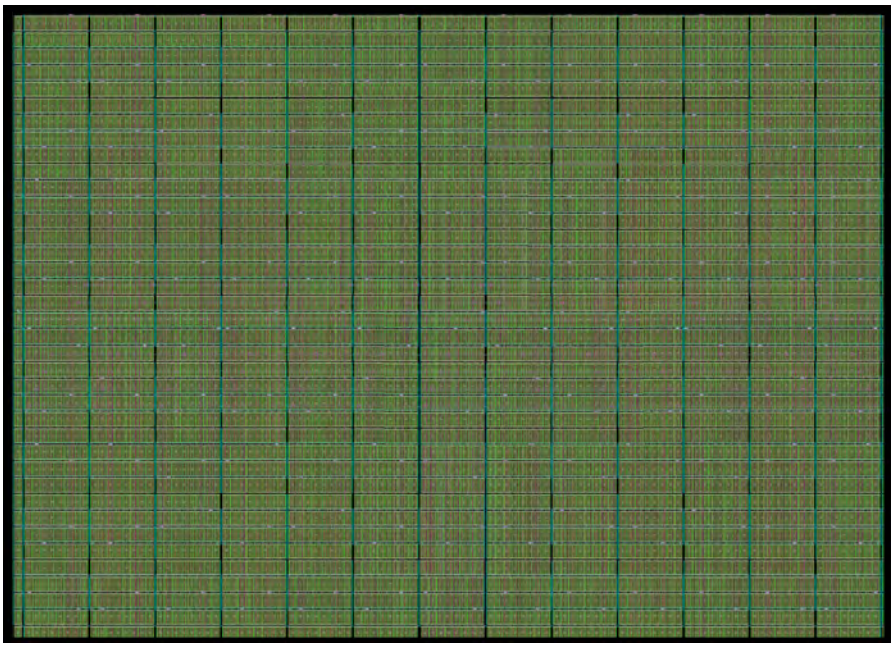

Figure 52: Layout of the capacitor block. The image shows a 650 µm by 450 µm area.

4.2 Operational Amplifier

The layout of the operational amplifier is implemented as the three transistor blocks listed below:

- *Upper current mirror*: Includes transistors M_{1a}, M_{1b} and M_4.
- *Lower current mirror*: Includes transistors M_{3a}, M_{3b}, M_{3c}, M_6 and M_5.

- *Differential pair*: Includes transistors M_{2a} and M_{2b}.

The upper current mirror block is implemented using the matching array shown in Figure 53 to ensure that the current copy is precise. Transistor M_4 does not belong to the current mirror but it is added to the array since it shares dimensions with M_{1a} and M_{1b}. No dummy devices are used for this arrangement as all transistors are surrounded by the bulk contact guard rings.

C	C	A	B	C	A	C	C	A	B
A	B	C	C	B	C	A	B	C	C

Figure 53: Transistor array for the upper current mirror. M_{1a}, M_{1b} and M_4 are represented by the letters A, B and C, respectively.

The layout of the lower current mirror is designed following the matching array of Figure 54. Transistors M_{3a}, M_{3b}, M_{3c} and M_6 are arranged with a common centroid. M_5 is used to implement the common-drain amplifier and therefore does not need to be matched in this array. Additionally, dummy transistors are placed at the top and bottom of this cell where there is no surrounding guard ring.

F	F	F	F	F
D	C	B	A	E
B	A	D	C	E
C	D	A	B	E
A	B	C	D	E
F	F	F	F	F

Figure 54: Transistor array for the lower current mirror. M_{3a}, M_{3b}, M_{3c}, M_6 and M_5 are represented by the letters A, B, C, D and E, respectively. The dummy transistors are indicated with the letter F.

On the other hand, the transistors of the differential pair are interdigitated for routing simplicity. The arrangement is shown in Figure 55 where dummy transistors are placed to the sides.

C	A	B	A	B	A	B	A	B	A	B	A	B	C

Figure 55: Transistor array for the differential pair. M_{2a} and M_{2b} are represented by the letters A and B, respectively. The dummy transistors are indicated with the letter C.

The layout of the operational amplifier is presented in Figure 56. The upper current mirror is located at the top, the differential pair is placed at the bottom left with the lower current mirror to its right. The total area is $1400\,\mu m^2$.

4.3 Switches

The layout for the switches is shown in Figure 57. The NMOS and PMOS transistors that comprise the TG are arranged along with the inverter from Figure 36.

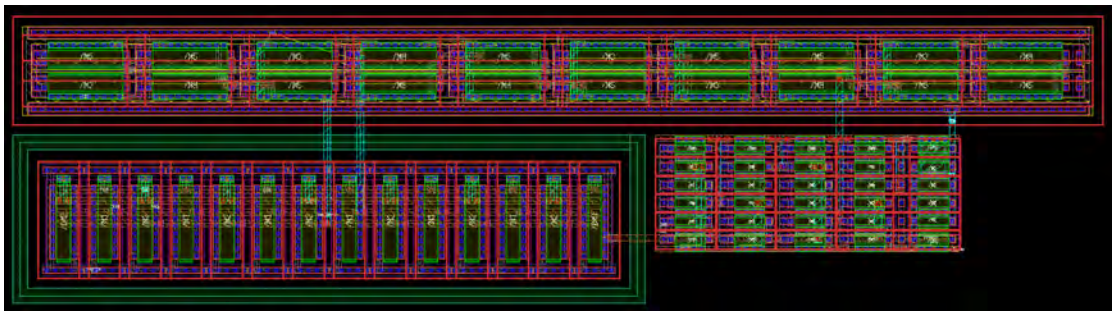

Figure 56: Transistor layout of the operational amplifier. The compensation capacitor is implemented within the capacitor block. The image shows a 75 µm by 20 µm area.

The area of each switch is 36 µm^2.

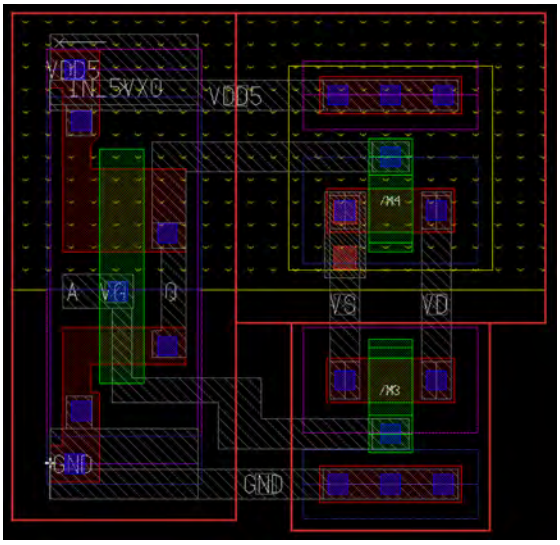

Figure 57: Layout of the TG and inverter circuit from Figure 36. The image shows a 6 µm by 6 µm area.

4.4 Digital Block

The digital block from Figure 42 is implemented using logic gates and a positive-edge triggered D flip-flop from the D_CELLS_5V library. The layout designed is presented in Figure 58 and has an area of 730 µm^2.

4.5 Pads and Buffers

The layouts of each block were routed together to complete the design of the SC amplifier. The input and output pads were selected and the simulation of the circuit was repeated.

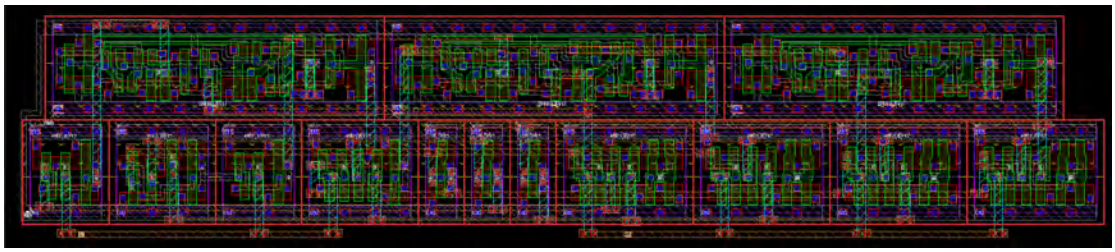

Figure 58: Layout of the digital block from Figure 42 The image shows a 61 µm by 12 µm area.

A few modifications were implemented to improve the performance of the module with the pads. These additions are depicted in Figure 59.

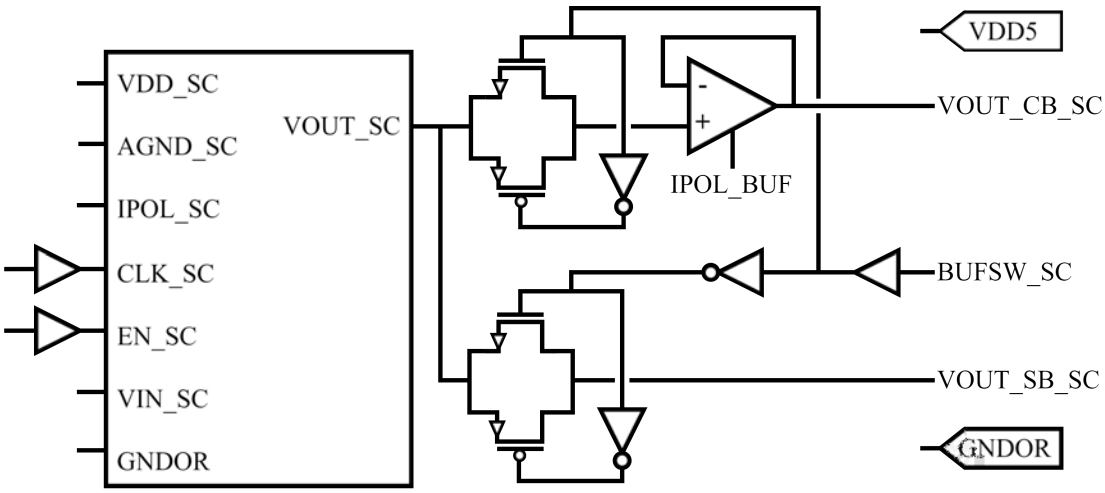

Figure 59: Modifications to the calibration module after adding the pads. The original module is represented by the block with its inputs and outputs. VDD5 is the voltage supply used for the additional components.

Digital buffers were added to the clock (CLK_SC) and enable (EN_SC) inputs. On the other hand, the circuit's output was buffered using a copy of the operational amplifier designed. For testing purposes, the output without the buffer was also left as a separate pin. TGs were placed to select either of these outputs (VOUT_CB_SC or VOUT_SB_SC) with the digital input BUFSW_SC. Since these additions are not strictly a part of the calibration module, they were designed to use a separate 5 V supply (VDD5).

The simulation was repeated after including these components and the results are presented in Figure 60. It can be seen that the errors are similar to those of section 3.6.7 (Final Design). The simulations were performed by activating and measuring the VOUT_CB_SC output.

The final layout of the calibration module is shown in Figure 61. The total area of the module without pads and the additional components of Figure 59 is 0.297 mm^2. This represents an 87% of the maximum area specified for the module. The outer dimensions are 636 µm by 481 µm.

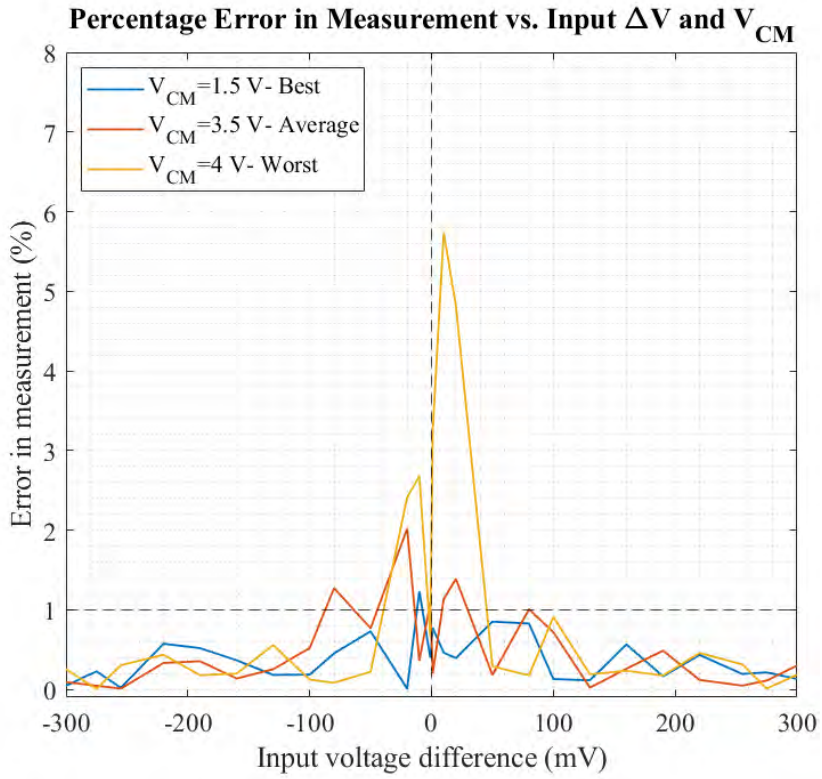

Figure 60: Simulation results of the SC amplifier including the additional components and pads. The input V_{CM} and ΔV used in the simulations are indicated in Table 17. The best, average and worst results from these simulations are presented in the plot.

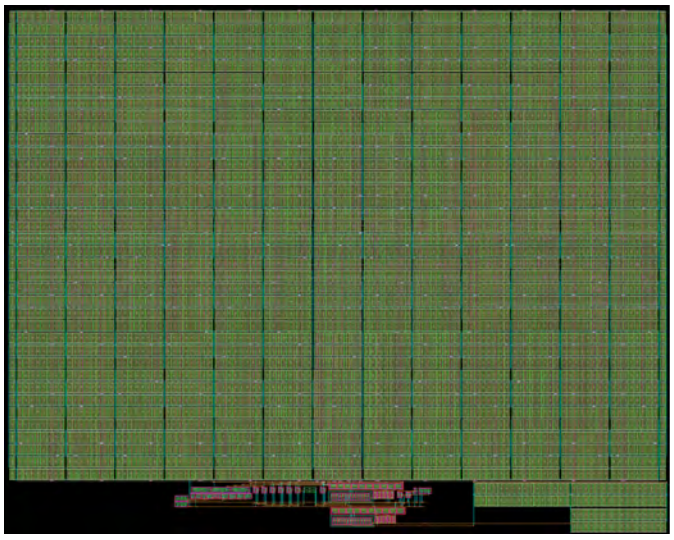

Figure 61: Final layout of the calibration module and the additional testing components. The image shows a 640 µm by 510 µm area.

4.6 Complete Chip

The calibration module was placed within the pad ring of a mini ASIC block and routed to its corresponding pads as shown in Figure 62. The chip was submitted for manufacturing in XFAB's XT018 180 nm CMOS technology in November 2021.

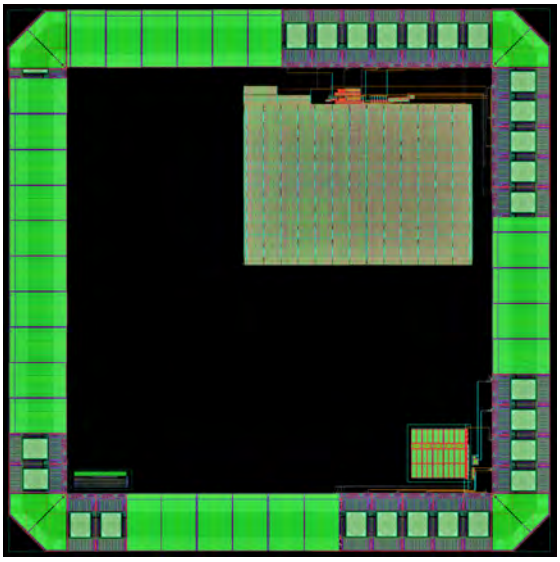

Figure 62: Final layout of the chip including the calibration module at the top right corner. The chip is a mini ASIC block with dimensions 1.52 mm x 1.52 mm.

Figure 63 shows the inputs and outputs of the calibration module. A Dual In-Line (DIL) 40 package is selected for the chip and the bonding diagram is shown in Figure 64. The pin numbers and pad models are listed in Table 19.

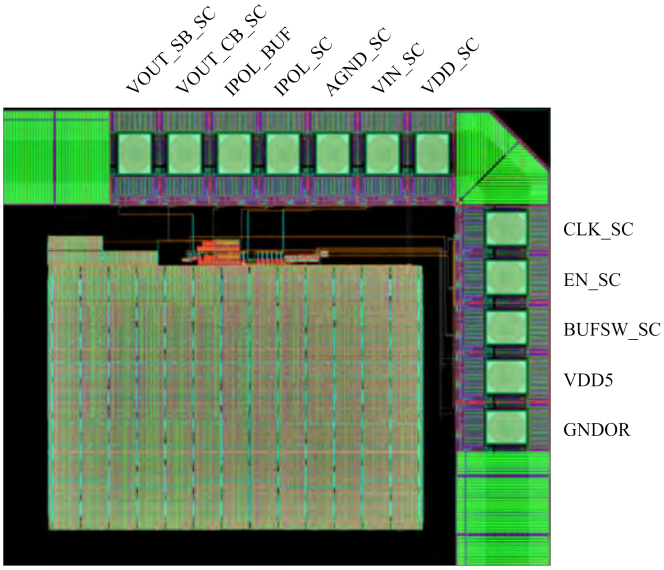

Figure 63: Layout of the calibration module with its input and output pads.

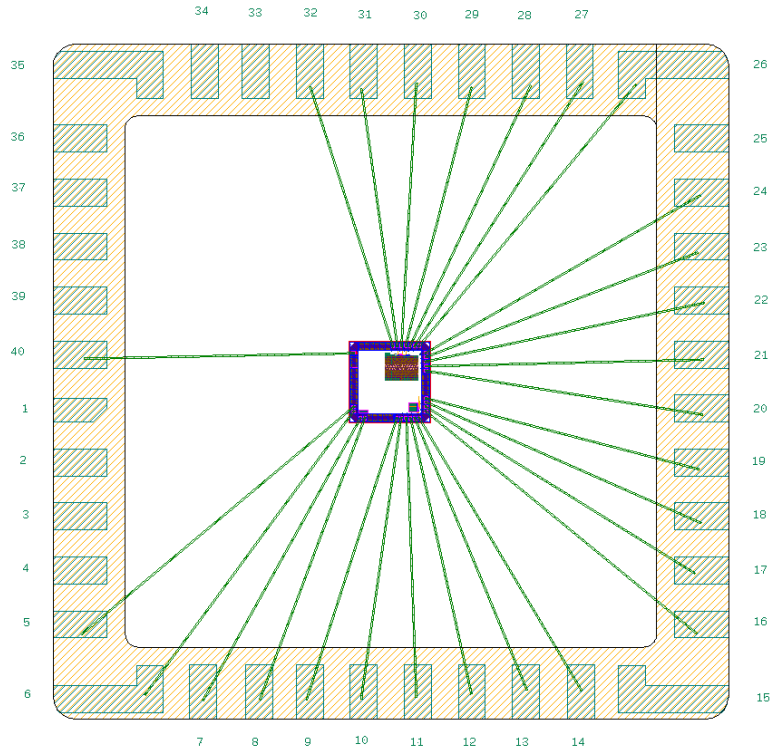

Figure 64: Bonding diagram for the IC of Figure 62 and a DIL 40 package.

Pin Name	**Pin No.**	**Pin Type**	**Description**	**Pad Type**
VOUT_SB_SC	32	Analog Output	Output	APR15DFC
VOUT_CB_SC	31	Analog Output	Buffered output	APR15DFC
IPOL_BUF	30	Analog Input	Bias current input for the output buffer	APR15DFC
IPOL_SC	29	Analog Input	Bias current input	APR15DFC
AGND_SC	28	VDD	AGND signal	VDDIPADFC
VIN_SC	27	Analog Input	Input to the calibration module	APR15DFC
VDD_SC	26	VDD	VDD	VDDIPADFC
CLK_SC	24	Digital Input	Clock signal	ICFC
EN_SC	23	Digital Input	Enable signal	ICFC
BUFSW_SC	22	Digital Input	Enable output buffer	ICFC
VDD5R	21	Digital Input	VDD for the buffer	VDD5PADFC
GNDOR	20	GND	Ground	GNDROPADF

Table 19: List of inputs and outputs of the calibration module along with their pad model and the corresponding pin number in the package. The input pin GNDOR is shared with the other two projects designed in the same chip.

Part 5

Setup for the Characterization of the Calibration Module

In this section, the measurement setup and steps to test the calibration module are proposed.

5.1 Measurement and Operation Setup

The following equipment is necessary to implement the measurement setup for the calibration module:

- A 5 VDC and a 1.65 VDC voltage source. An additional DC voltage source capable of providing an output up to 5 V may be used for the first testing phase as described in section 5.2 (Measurement Plan).
- A 500 nA and a 3 µA current source or SMU.
- An external MCU with at least 3 GPIOs available driven by 5 VDC.
- An oscilloscope with a bandwidth of at least 10 MHz and a precision of 1 mV.
- To model the input to the module: The second version of the current source or an IC with an adjustable current/voltage source, a 1 µF capacitor and a set of resistors or SMU.

The general setup for the characterization of the calibration module is depicted in Figure 65.

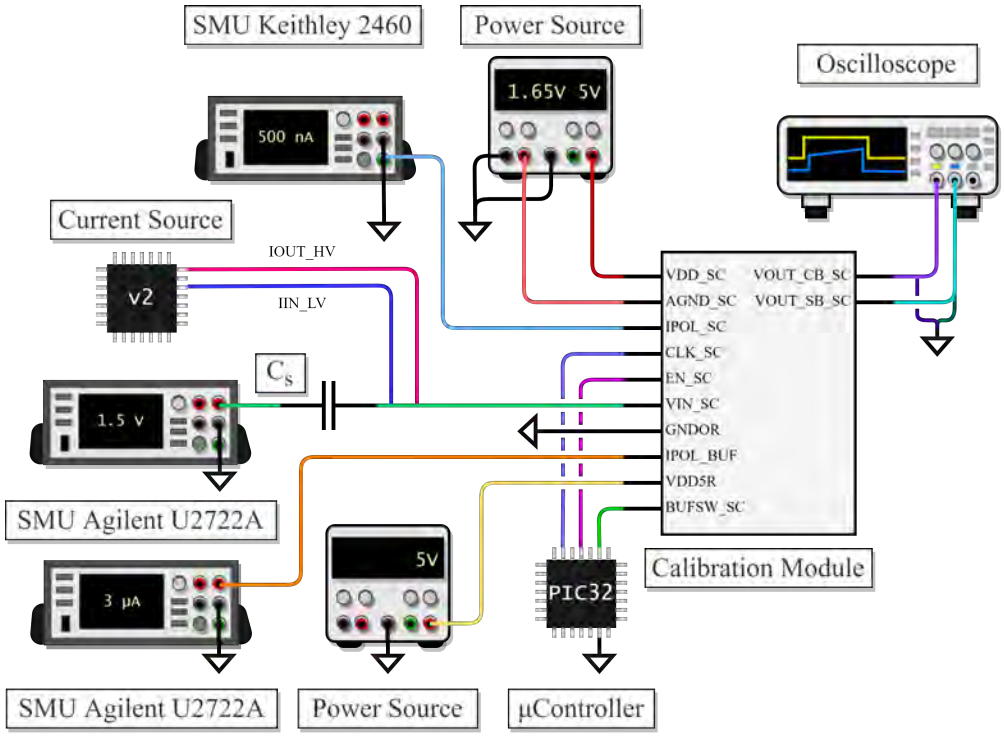

Figure 65: Setup for the characterization of the calibration module.

As shown in Figure 65, either of the outputs (VOUT_CB_SC or VOUT_SB_SC) is connected to an oscilloscope. To measure the buffered output VOUT_CB_SC,

the BUFSW_SC pin should be driven high whereas a low input to BUFSW_SC would activate the unbuffered output VOUT_SB_SC.

In this testing phase an external MCU is used to program the digital inputs to the module (CLK_SC and EN_SC). Figure 66 shows the required timing to trigger these signals and the current sources.

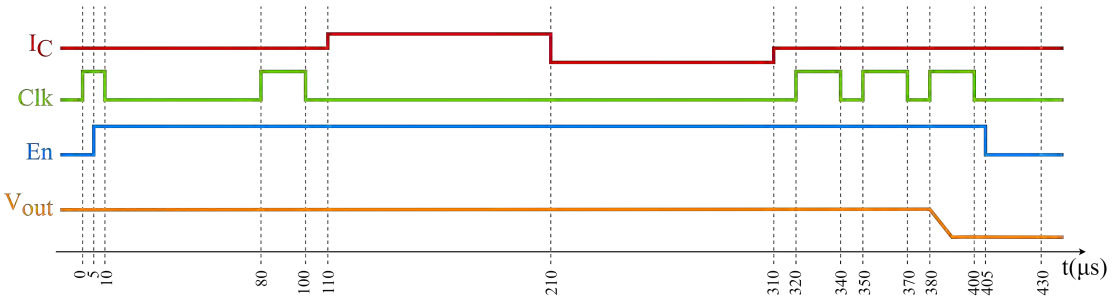

Figure 66: Timing diagram for the calibration module. The waveforms show the delays and pulse widths for the current source stimulation (I_C) and the enable and clock digital inputs. The valid output of the calibration module is generated 430 µs after triggering the clock signal.

In order to model the analog input to the calibration module (VIN_SC) there are three options that may be implemented in different stages of the testing phase:

1. Connecting an adjustable voltage source IC to the VIN_SC input that models the combined effect of the current sources, safety capacitor and tissue resistance.

2. Connecting an adjustable current source IC to generate the stimulation pulses, the 1 µF safety capacitor and an appropriate resistor or an SMU to model the voltage drop across the tissue.

3. Connecting the chip with the second version of the current source, the 1 µF safety capacitor and an appropriate resistor or an SMU to model the voltage drop across the tissue. The setup for the second version of the current source is implemented as described in section 2.2.1.2 (Second Version).

For the first option, the voltage source IC should have an output in the 0 to 5 V range, a 1 mV resolution and a settling time of about 10 µs. The DAC8512 by Analog Devices [36] or the MCP4725 [37] by Microchip Technology may be used. The DAC8512 is a 12-bit voltage Digital-to-Analog Converter (DAC) with an output range from 0 to 4.095 V, 1 mV steps, a ±1 mV typical error and a settling time of 16 µs for an output precision of ±1 mV. The MCP4725 is also a 12-bit voltage DAC with the same step size and output range, a ±2.2 mV typical error, a settling time of 10 µs for an output precision of ±1 mV. The MCP4725 can also be purchased with a breakout board.

For the second option, the current source IC should have a 0 to 25.5 mA output range with 100 µA steps, a typical error of less than 1% and a settling time of about 10 µs. The CY8C4014FNI-421 by Infineon Technologies [38] may be used

for this purpose. It is a Programmable System-on-Chip (PSoC) with an 8-bit and a 7-bit current Current Digital-to-Analog Converter (IDAC). The output can range from 0 to 612 µA and 304.8 µA, respectively. Both integrated IDACs have a maximum error of ±9.5 µA and a settling time of 10 µs for a ±1.2 µA error. They are easily programmable through a graphic interface. However, this specific IC would only allow to test the lower current levels. For higher currents the second version of the current source would be necessary.

Prior to connecting the VIN_SC input it is necessary to ensure that the voltage will remain within the 0 to 5 V range as indicated in the following section.

5.2 Measurement Plan

Once the setup of Figure 65 is implemented and the timing shown in Figure 66 is programmed in the external MCU, the measurements can be performed.

If all inputs but EN_SC and CLK_SC are activated and set to their nominal values, and the VIN_SC input is set to a constant voltage in the 0 to 5 V range, the output of the calibration module should read 0 V. For simplicity, in this testing step the constant input voltage for VIN_SC may be generated by a standard DC voltage source. Once EN_SC and CLK_SC are programmed and the VIN_SC input is kept fixed at a constant voltage between 0 and 5 V, the measured output should be close to AGND. This step ensures that the blocks are working properly by emulating a CDS run.

The next test involves characterizing the stimulation run which may be done in two different steps.

The first step requires either a current or a voltage source IC to model the VIN_SC input.

If a voltage source is available, it can be programmed to be applied directly to the module without connecting the safety capacitor or the tissue resistance. Initially (i.e., during the first 110 µs in Figure 66) the input can take up any value from 0 to 5 V. By 310 µs the input needs to be changed to a different voltage. The difference between these two values is ΔV from section 3.2 (Output Voltage Measurement).

The voltage output to the module is then measured and the experimental ΔV may be computed as indicated in Equation 20. The input and measured ΔV can be compared to characterize the operation of the calibration module. An example set of ΔV values is shown in Table 17.

On the other hand, if a current source IC is available, the pulses are programmed following the timing scheme of Figure 66. The current amplitudes may range from 100 µA up to 25.5 mA. The mismatch between the sinking and sourcing pulses should be set in the 1 to 10% range. A 1 µF safety capacitor is connected to the output as shown in Figure 28. The tissue resistance can be modeled using a resistor with a value such that the input voltage VIN_SC is between 0 and

5 V. The lower and upper bounds for the resistance can be set by repeating the analysis of section 3.2 (Output Voltage Measurement). The result is indicated in Equation 26 where V_{min} and V_{max} are 0 and 5 V, respectively and V_0 is the initial voltage prior to the stimulation.

$$\frac{V_{min} - V_0 - \frac{T}{2C_s} I_{source}}{I_{sink}} - \frac{T}{2C_s} < R < \frac{V_{max} - V_0}{I_{source}} - \frac{T}{2C_s} \tag{26}$$

Alternatively, the tissue resistance may be modeled as a constant voltage drop generated by an SMU or voltage source. The advantage of using an SMU is that the current from the IC can be measured simultaneously with the same instrument. The range of values for the SMU voltage (V_{SMU}) is defined by Equation 27.

$$V_{min} - V_0 - \frac{T}{2C_s} (I_{source} + I_{sink}) < V_{SMU} < V_{max} - V_0 - \frac{T}{2C_s} I_{source} \tag{27}$$

From the output voltage measurement, the difference between the sourcing and sinking current amplitudes, ΔI, can be computed using Equation 25 and then compared against the input difference.

It should also be verified that the output voltage to the module is independent of the tissue resistance. This can be achieved by repeating the measurements while changing the value of the resistor or SMU in the ranges defined by Equation 26 and Equation 27, respectively.

In this case, the current level and the current difference between both phases can be modified to take multiple measurements and characterize the operation of the module. This may include selecting 50 of the 256 current levels defined for the second version of the current source, generating a 1%, 5% and 10% mismatch between both phases and registering the measured output.

By default the buffered output (VOUT_CB_SC) should be selected and measured. As part of the testing phase, the unbuffered output (VOUT_SB_SC) can also be measured and used for comparison.

As the second testing step, the previous measurements can be repeated by setting up the second version of the current source and connecting it to the VIN_SC input with the safety capacitor and resistor or SMU to model the tissue. This would allow to test the performance of both designs combined. The trimming adjustment may also be performed to simulate the complete operation of the module.

Finally, the current consumption can be characterized by measuring the current through the 5 V source connected to the VDD_SC pin while the module is turned on and comparing it against the theoretical consumption of 1.5 µA.

Part 6

Conclusions

The scope of this project was divided into two main objectives for which the following conclusions are derived.

6.1 Characterization of the Integrated Programmable Current Sources

Both versions of the existing integrated programmable current sources were fully characterized and the results are presented in Part 2 (Characterization of the Integrated Programmable Current Sources).

The measured parameters include the output current range and level precision, the characterization of the trimming mechanism, the supply voltage range for both LV and HV inputs, the output voltage range, the bias current - output current relation, response times, current consumption and crosstalk between the sinking and sourcing phases.

The complete characterization of each version of the current source required using precision instruments, designing a PCB for the input and output connections, mounting the measurement setup and programming an external MCU to load the shift registers and select the stimulation amplitude, duration and trimming levels. The characterization process also involved the analysis of the data gathered from the measurements.

As can be seen in Table 6, the results allow to validate both designs and their respective specifications as well as detecting issues and testing the improvements implemented in the second version of the current source.

On the other hand, the complete performance of the trimming model was simulated from the data collected in section 2.2.3 (Simulated Trimming Model for Current Adjustment). The results show that the output current can be adjusted to a 1% precision by means of the trimming mechanism.

6.2 Design of the Calibration Module

An additional calibration module was designed to be appended to the second version of the current stimulator. It was implemented and submitted for manufacturing in XFAB's XT018 180 nm CMOS technology in November 2021.

The purpose of the calibration module is to measure the difference in the current amplitudes of the sourcing and sinking phases. The measurement is then processed by the CPU which adjusts the trimming levels to the current sources. By doing so the net charge transfer to the tissue can be reduced.

The module uses the CDS technique to eliminate the effect of the constant output offset by adding an extra step where no stimulation is performed. The complete calibration routine is described in Figure 39.

The design consists of an SC amplifier circuit (Figure 34) that uses a LV amplifier and switching capacitors to transfer charge around the circuit and generate an output related to the current mismatch.

The input to the module is the voltage at the current source's output where the safety capacitor is connected. Any mismatch in the sourcing and sinking currents will charge or discharge the safety capacitor changing the voltage at this node with every stimulation. By measuring this voltage difference and outputting it to the 12-bit ADC, the CPU can then compute the current difference from the module's output using Equation 25. Once the current mismatch is characterized, it can be corrected by adjusting the trimming bits.

The performance of the module is simulated and the resulting design specifications are summarized in Table 20. It can be seen that the calibration module complies with the input, output, area and typical precision requirements.

Specifications	
Output	Analog LV output related to current difference
Input	Analog input in the 0-5 V range
Area	0.297 mm^2
Timing	200 µs calibration pulse
Safety Capacitor	1 µF
Current consumption	1.5 µA
Duration of each activation	430 µs
Precision*	Typ.: 0.6%, Max.: 5.8%
Digital inputs	Clk and En signals with a fixed pattern
Activation	CDS iteration followed by calibration runs
Bias current	500 nA
AGND Voltage	1.65 V

Table 20: Design Specifications of the Calibration Module. *The precision was computed by finding the maximum and average of all simulated results from Table 17

The calibration module was designed to be easily adapted to HV inputs and to function as an ETI impedance measurement device as discussed in section 6.3.2 (Redesign for High Voltage) and section 6.3.3 (Module for Impedance Measurement), respectively.

From an academic point of view, this project has allowed to develop skills in areas such as analog and digital design, physical implementation of devices using CAD software, widely-followed layout practices, device characterization, instrument setup and calibration, measurement analysis, firmware and PCB development, IMDs and their requirements, research and documentation.

The project's original and executed roadmaps are presented in section 9.1 (Roadmap).

6.3 Future Work

The following subsections include areas to improve and work on during future design stages.

6.3.1 Improvements to the Calibration Module

The output's precision is an area that can yet be investigated and improved upon.

Although the ideal simulations had shown that the error was negligible, once the design blocks were implemented it was found that the precision of the module is sensitive to the input common mode voltage. Later simulations showed that this is particularly the case when the change in input voltage following the stimulation pulse is less than 20 mV. Here the precision is usually of around 2% or higher. Even though an ideal value would be 1%, a precision of around 5% would still be improving the mismatch that the sources currently have for the lower levels as measured in section 2.2.2.2 (Output Current Range). It should also be noted that the specific application of the stimulator will ultimately determine the real threshold values.

6.3.2 Redesign for High Voltage

As mentioned in section 3.3 (Operation Requirements), the technology available to implement the project does not include transistors with a HV V_{GS}. This would be necessary to control the TGs if the voltage input to the module is between 5 V and 15 V.

The module was designed to be easily adapted to high voltage inputs only by changing the TGs. The capacitors selected for the design can handle up to 60 V and the LV amplifier is compatible with a HV input due to the use of the floating capacitor.

6.3.3 Module for Impedance Measurement

An additional functionality to integrate to the current stimulator is the measurement of the ETI impedance. Changes in the value of this impedance may be indicative of complications such as tissue edema, poor electrode connection or lead malfunction [1]. All of these issues impact the stimulation and thus it is essential that they are detected on time.

The same SC amplifier topology and working principle used in the calibration design may be applied to implement the impedance measurement module. Instead of sampling the voltages prior to and following the stimulation, the impedance module would sample the input half a period into the sourcing and sinking phases as illustrated in Figure 67.

The analysis of section 3.2 (Output Voltage Measurement) can be repeated to determine the relation between the samples and the ETI impedance. Assuming

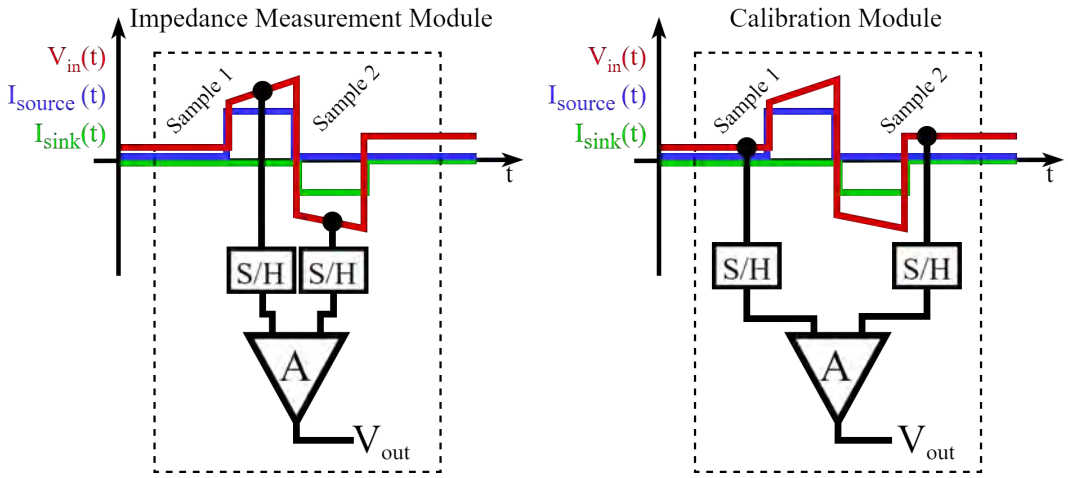

Figure 67: Operation of the impedance measurement device (left) and the calibration module (right). The illustration shows the instants at which the input is sampled. The CDS run was omitted for simplicity.

that the sourcing and sinking phases are matched by previously activating the calibration module, I_{source} and $-I_{sink}$ can be simplified as $I_{nominal}$. Thus, the difference in voltage between the samples (ΔV_R) and the ETI impedance (modelled by a resistance R) are related by Equation 28.

$$R = \frac{\Delta V_R}{2I_{nominal}} \tag{28}$$

The ETI impedance can be determined from the module's output (V_{out}) using Equation 29.

$$R = \frac{V_{out} - V_{AGND}}{2GI_{nominal}} \tag{29}$$

While the calibration module was designed to detect voltage input differences on the order of tens of mV, the impedance measurement circuit must be capable of measuring differences of a few V. To keep the amplifier from saturating, a single module capable of successfully performing both functionalities requires an adaptive gain. Given that the gain of the SC amplifier is determined by the capacitance values (Equation 17) this could be simply done by adding switches that select different sets of capacitors for each task.

Therefore, the module would first perform a current calibration routine and then take samples to measure the ETI impedance. The measured output would be stored on the chip's memory to compare against the subsequent measurements, thus monitoring the changes in the impedance value over time.

Part 7

Acronyms

ACM Advanced Compact MOSFET. 59

ADC Analog-to-Digital Converter. 40, 45, 46, 50, 82

ASIC Application-Specific Integrated Circuit. 18, 19, 73

CAD Computer-Aided Design. 44, 82

CDS Correlated Double Sampling. 46, 54, 55, 56, 63, 64, 78, 81, 84

CMOS Complementary Metal-Oxide-Semiconductor. 52

CPU Central Processing Unit. 12, 14, 15, 19, 22, 39, 45, 65, 81, 82

DAC Digital-to-Analog Converter. 77

DC Direct Current. 17, 21, 22, 26, 54, 76, 78

DIL Dual In-Line. 73, 74

EMI Electromagnetic Interference. 22

ESD Electrostatic Discharge. 24

ETI Electrode-Tissue Interface. 3, 13, 14, 17, 46, 82, 83, 84

FSM Finite-State Machine. 56, 57, 58

GPIO General-Purpose Input/Output. 21, 22, 76

HV High Voltage. 17, 18, 19, 44, 45, 47, 51, 81, 82, 83

IC Integrated Circuit. 35, 76, 77, 78, 79

IDAC Current Digital-to-Analog Converter. 78

IMD Implantable Medical Device. 3, 12, 13, 82

LV Low Voltage. 17, 18, 19, 40, 44, 47, 65, 81, 82, 83

MCU Microcontroller Unit. 21, 22, 23, 24, 76, 77, 78, 81

MI Moderate Inversion. 60

OTA Operational Transconductance Amplifier. 103, 104

PCB Printed Circuit Board. 20, 22, 23, 81, 82, 101, 102

PSoC Programmable System-on-Chip. 78

RC Resistor-Capacitor. 13

RISC Reduced Instruction Set Computing. 14, 93

SC Switched-Capacitor. 3, 46, 47, 48, 49, 51, 52, 54, 56, 64, 70, 72, 82, 83, 84

SI Strong Inversion. 60

SMU Source Measure Unit. 21, 22, 24, 34, 76, 77, 79

SOI Silicon-On-Insulator. 18

TG Transmission Gate. 52, 53, 54, 55, 56, 69, 70, 71, 83

UART Universal Asynchronous Receiver-Transmitter. 93

USB Universal Serial Bus. 93

WI Weak Inversion. 60

Part 8

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Part 9

Annex

9.1 Roadmap

The roadmap planned for this project is portrayed in Figure 68 and it is compared against the actual execution of each task. The original and executed schedules show only slight variations. The RISC-V firmware development was compromised to invest more time in the full characterization of both versions of the current sources and measurement analysis. On the other hand, the completion of the layout was prioritized over the documentation process during the months of September and October since the deadline for fabrication submission was November 10th.

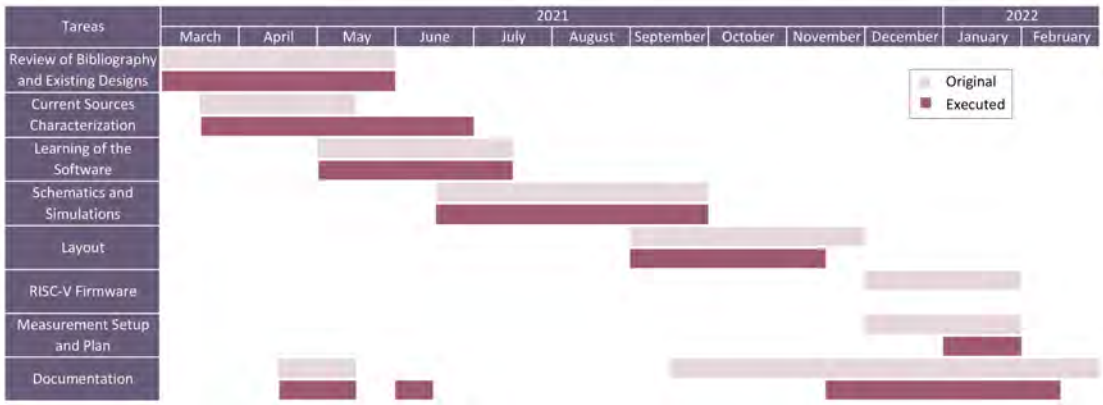

Figure 68: Roadmap comparison of the original and executed plans.

9.2 Firmware for the Microcontroller

In this section, the main programming code used to characterize the current sources is presented. It was written in C and compiled using MPLAB's XC32 Compiler Version 2.20.

The firmware implements the stimulation sequence that sets the output current and the duration of the pulses. This is done by loading the programming and trimming bits into a shift register and also setting the bits that enable either the sinking or sourcing phases. The routine also generates the clock signal necessary to load the register and the trigger signal that commands the stimulation pulse.

The user interface was implemented using the Universal Asynchronous Receiver-Transmitter (UART) connected to a computer terminal through the Universal Serial Bus (USB) port. This allowed the user to input the desired current and trimming levels as well as selecting whether the sinking or sourcing phase is enabled.

Extract 1: Code extract implemented to test the second version of the current source.

```
#include "app.h"

static uint8_t r_current_b[ ] = {0, 1, 2, 3, 4, 5, 6, 7};
static uint8_t r_trimming_drain_b[ ] = {11, 12, 13, 14, 15};
```

```
static uint8_t r_trimming_source_b[ ] = {19, 20, 21, 22, 23};
static uint8_t r_EN_drain = 28;
static uint8_t r_EN_source = 29;
static uint8_t r_bit_test = 33;
static uint8_t registro[APP_SIZE_REGISTRO] = {0};
static uint8_t reverse_registro[APP_SIZE_REGISTRO] = {0};
static uint8_t current_byte;

void reverse(uint8_t* arr, uint8_t* aux, uint32_t n) {
    uint32_t i;

    for (i = 0; i < n; i++) {
        aux[n - 1 - i] = arr[i];
    }
}

void triggerStimulation() {
    uint32_t i;

    for (i = 0; i < sizeof (r_current_b); i++) {
        if ((current_byte >> i) & 1 == 1) {
            registro[r_current_b[i]] = 1;
        } else {
            registro[r_current_b[i]] = 0;
        }
    }
    for (i = 0; i < sizeof (r_current_b); i++) {
        if ((current_byte >> i) & 1 == 1) {
            registro[r_current_b[i]] = 1;
        } else {
            registro[r_current_b[i]] = 0;
        }
    }

    registro[r_bit_test] = 1;

    //Reset register
    RESET_N_SetLow();
    DELAY_us(100);
    RESET_N_SetHigh();

    //Reverse register before loading
    reverse(registro, reverse_registro, APP_SIZE_REGISTRO);

    for (i = 0; i < APP_SIZE_REGISTRO; i++) {
        if (reverse_registro[i] == 1) {
            DATA_IN_SetHigh();
        } else {
            DATA_IN_SetLow();
        }
        DELAY_us(75);
        CLK_SetHigh();
        DELAY_us(75);
        CLK_SetLow();
    }
```

```
60      DELAY_us(10000);
61      //Trigger activation
62      TRIGGER_SetHigh();
63      DELAY_us(APP_PULSE_WIDTH_US);
64      TRIGGER_SetLow();
65  }
66
67  APP_STIMULATION_STATUS_t APP_bitStimulationFCD() {
68      static uint8_t currentInput;
69      static uint8_t stateSingle = APP_STIMULATION_INIT;
70
71      switch (stateSingle) {
72          case APP_STIMULATION_INIT:
73              memset(registro, 0, APP_SIZE_REGISTRO);
74              memset(reverse_registro, 0, APP_SIZE_REGISTRO);
75              RESET_N_SetHigh();
76              CLK_SetLow();
77              DATA_IN_SetLow();
78              TRIGGER_SetLow();
79              //Load trimming bits
80              registro[r_trimming_drain_b[0]] = 1;
81              registro[r_trimming_drain_b[1]] = 1;
82              registro[r_trimming_drain_b[2]] = 0;
83              registro[r_trimming_drain_b[3]] = 0;
84              registro[r_trimming_drain_b[4]] = 1;
85              USB_write("\n Fuente de corriente a tierra\n");
86              USB_write("\n  Ingresar nivel de corriente (entre 1 y
    255)\n");
87
88              stateSingle = APP_STIMULATION_WAIT;
89              break;
90
91          case APP_STIMULATION_WAIT:
92              strcpy(USB_dummyBuffer, USB_read(0));
93              currentInput = (uint8_t) strtol((char*)
    USB_dummyBuffer, NULL, 10);
94              if (currentInput>0 && currentInput<=255) {
95                      USB_write("\n      ...Valor correcto\n");
96                      current_byte = currentInput;
97                      registro[r_EN_drain] = 1;
98                      registro[r_EN_source] = 0;
99                      stateSingle = APP_STIMULATION_VALIDATE;
100             }
101             break;
102
103         case APP_STIMULATION_VALIDATE:
104             triggerStimulation();
105             stateSingle = APP_STIMULATION_INIT;
106             return APP_STIMULATION_RETURN;
107
108         default: break;
109     }
110     return APP_STIMULATION_WORKING;
111 }
112
```

```
APP_STIMULATION_STATUS_t APP_bitStimulationFCF() {
    static uint8_t currentInput;
    static uint8_t stateSingle = APP_STIMULATION_INIT;

    switch (stateSingle) {
        case APP_STIMULATION_INIT:
            memset(registro, 0, APP_SIZE_REGISTRO);
            memset(reverse_registro, 0, APP_SIZE_REGISTRO);
            RESET_N_SetHigh();
            CLK_SetLow();
            DATA_IN_SetLow();
            TRIGGER_SetLow();
            //Load trimming bits
            registro[r_trimming_source_b[0]] = 1;
            registro[r_trimming_source_b[1]] = 1;
            registro[r_trimming_source_b[2]] = 1;
            registro[r_trimming_source_b[3]] = 1;
            registro[r_trimming_source_b[4]] = 0;

            USB_write("\n Fuente de corriente a tejido\n");
            USB_write("\n Ingresar nivel de corriente (entre 1 y
    255)\n");

            stateSingle = APP_STIMULATION_WAIT;
            break;

        case APP_STIMULATION_WAIT:
            strcpy(USB_dummyBuffer, USB_read(0));
            currentInput = (uint8_t) strtol((char*)
    USB_dummyBuffer, NULL, 10);
            if (currentInput>0 && currentInput<=255) {
                    USB_write("\n      ...Valor correcto\n");
                    current_byte = currentInput;
                    registro[r_EN_drain] = 0;
                    registro[r_EN_source] = 1;
                    stateSingle = APP_STIMULATION_VALIDATE;
            }
            break;

        case APP_STIMULATION_VALIDATE:
            triggerStimulation(); //Single trigger
            stateSingle = APP_STIMULATION_INIT;
            return APP_STIMULATION_RETURN;

        default: break;
    }
    return APP_STIMULATION_WORKING;
}

APP_STIMULATION_STATUS_t APP_trimmingStimulationBitsDrain() {
    static uint8_t trimmingInput;
    static uint8_t stateTrimming = APP_STIMULATION_INIT;
    uint32_t i;
    uint8_t TRIMMING_byte;

```

```
166     switch (stateTrimming) {
167         case APP_STIMULATION_INIT:
168             memset(registro, 0, APP_SIZE_REGISTRO);
169             memset(reverse_registro, 0, APP_SIZE_REGISTRO);
170             RESET_N_SetHigh();
171             CLK_SetLow();
172             DATA_IN_SetLow();
173             TRIGGER_SetLow();
174 
175             USB_write("\n Simulacion de trimming para fuente Drain
    con una corriente fija\n");
176             USB_write(" Ingresar nivel de trimming (de 0 a 31)\n");
177             stateTrimming = APP_STIMULATION_WAIT;
178             break;
179 
180         case APP_STIMULATION_WAIT:
181             strcpy(USB_dummyBuffer, USB_read(0));
182             trimmingInput = (uint8_t) strtol((char*)
    USB_dummyBuffer, NULL, 10);
183             if (trimmingInput > 0 && trimmingInput <= 31) {
184                 USB_write("\n      ...Valor correcto\n");
185                 current_byte = 255;
186                 registro[r_EN_drain] = 1;
187                 registro[r_EN_source] = 0;
188 
189                 TRIMMING_byte = trimmingInput;
190                 //Load trimming bits
191                 registro[r_trimming_drain_b[0]] = TRIMMING_byte &
    1;
192                 registro[r_trimming_drain_b[1]] = TRIMMING_byte >>
    1 & 1;
193                 registro[r_trimming_drain_b[2]] = TRIMMING_byte >>
    2 & 1;
194                 registro[r_trimming_drain_b[3]] = TRIMMING_byte >>
    3 & 1;
195                 registro[r_trimming_drain_b[4]] = TRIMMING_byte >>
    4 & 1;
196 
197                 stateTrimming = APP_STIMULATION_VALIDATE;
198             }
199             break;
200 
201 
202         case APP_STIMULATION_VALIDATE:
203             triggerStimulation();
204             stateTrimming = APP_STIMULATION_INIT;
205             return APP_STIMULATION_RETURN;
206 
207         default: break;
208     }
209     return APP_STIMULATION_WORKING;
210 }
211 
212 APP_STIMULATION_STATUS_t APP_trimmingStimulationBitsSource() {
213     static uint8_t trimmingInput;
```

```
214     static uint8_t stateTrimming = APP_STIMULATION_INIT;
215     uint32_t i;
216     uint8_t TRIMMING_byte;
217 
218     switch (stateTrimming) {
219         case APP_STIMULATION_INIT:
220             memset(registro, 0, APP_SIZE_REGISTRO);
221             memset(reverse_registro, 0, APP_SIZE_REGISTRO);
222             RESET_N_SetHigh();
223             CLK_SetLow();
224             DATA_IN_SetLow();
225             TRIGGER_SetLow();
226 
227             USB_write("\n Simulacion de trimming para fuente
    Source con una corriente de 25mA (nivel 255)\n");
228             USB_write(" Ingresar nivel de trimming (de 0 a 31)\n");
229             stateTrimming = APP_STIMULATION_WAIT;
230             break;
231 
232         case APP_STIMULATION_WAIT:
233             strcpy(USB_dummyBuffer, USB_read(0));
234             trimmingInput = (uint8_t) strtol((char*)
    USB_dummyBuffer, NULL, 10);
235 
236             if (trimmingInput > 0 && trimmingInput <= 31) {
237                 USB_write("\n      ...Valor correcto\n");
238                 current_byte = 255;
239                 registro[r_EN_drain] = 0;
240                 registro[r_EN_source] = 1;
241                 TRIMMING_byte = trimmingInput;
242                 //Load trimming bits
243                 registro[r_trimming_source_b[0]] = TRIMMING_byte &
    1;
244                 registro[r_trimming_source_b[1]] = TRIMMING_byte
    >> 1 & 1;
245                 registro[r_trimming_source_b[2]] = TRIMMING_byte
    >> 2 & 1;
246                 registro[r_trimming_source_b[3]] = TRIMMING_byte
    >> 3 & 1;
247                 registro[r_trimming_source_b[4]] = TRIMMING_byte
    >> 4 & 1;
248                 stateTrimming = APP_STIMULATION_VALIDATE;
249             }
250             break;
251 
252         case APP_STIMULATION_VALIDATE:
253             triggerStimulation();
254             stateTrimming = APP_STIMULATION_INIT;
255             return APP_STIMULATION_RETURN;
256 
257         default: break;
258     }
259     return APP_STIMULATION_WORKING;
260 }
261 
```

```
262 void APP_UI() //User interface
263 {
264     static uint8_t UI_STATE = APP_UI_STATE_INIT;
265     static uint8_t retMenu;
266 
267      switch (UI_STATE) {
268         case APP_UI_STATE_INIT:
269 
270             USB_write("\n\n\n--------Simulacion estimulo
    tejido--------\n\n");
271             USB_write("    ->Presionar '1' para programar un pulso
    con la fuente Drain\n");
272             USB_write("    ->Presionar '2' para programar un pulso
    con la fuente Source\n");
273             USB_write("    ->Presionar '3' para simular trimming
    de la fuente Drain\n");
274             USB_write("    ->Presionar '4' para simular trimming
    de la fuente Source\n");
275             UI_STATE = APP_UI_STATE_MENU_SHOW;
276             break;
277 
278         case APP_UI_STATE_MENU_SHOW:
279             strcpy(USB_dummyBuffer, USB_read(0));
280             retMenu = (uint8_t) strtol((char*) USB_dummyBuffer,
    NULL, 10);
281             switch (retMenu) {
282 
283                 case 1:
284                     USB_write("\n      ...Generar pulso de
    corriente (fuente Drain)\n");
285                     UI_STATE = APP_UI_STATE_BITS_FCD;
286                     break;
287 
288                 case 2:
289                     USB_write("\n      ...Generar pulso de
    corriente (fuente Source)\n");
290                     UI_STATE = APP_UI_STATE_BITS_FCF;
291                     break;
292 
293                 case 3:
294                     USB_write("\n      ...Simular trimming (fuente
    Drain)\n");
295                     UI_STATE = APP_UI_STATE_TRIMMING_BITS_DRAIN;
296                     break;
297 
298                 case 4:
299                     USB_write("\n      ...Simular trimming (fuente
    Source)\n");
300                     UI_STATE = APP_UI_STATE_TRIMMING_BITS_SOURCE;
301                     break;
302 
303                 default: break;
304             }
305             break;
306 
```

```
307
308         case APP_UI_STATE_BITS_FCD:
309             if (APP_bitStimulationFCD()) {
310                 USB_write("\n      ...Ejecucion finalizada\n");
311                 UI_STATE = APP_UI_STATE_INIT;
312             }
313             break;
314
315         case APP_UI_STATE_BITS_FCF:
316             if (APP_bitStimulationFCF()) {
317                 USB_write("\n      ...Ejecucion finalizada\n");
318                 UI_STATE = APP_UI_STATE_INIT;
319             }
320             break;
321
322         case APP_UI_STATE_TRIMMING_BITS_DRAIN:
323             if (APP_trimmingStimulationBitsDrain()) {
324                 USB_write("\n      ...Ejecucion finalizada\n");
325                 UI_STATE = APP_UI_STATE_INIT;
326             }
327             break;
328
329         case APP_UI_STATE_TRIMMING_BITS_SOURCE:
330             if (APP_trimmingStimulationBitsSource()) {
331                 USB_write("\n      ...Ejecucion finalizada\n");
332                 UI_STATE = APP_UI_STATE_INIT;
333             }
334             break;
335
336     }
337
338 }
```

The code extract presented was used to test the second version of the current source. The firmware for the first version follows the same logic and structure. Besides the change in the trimming mechanism, there are a few changes to the array indexes for the shift register as shown in the extract below.

Extract 2: Code extract showing the difference in the array indexes for the shift register in the first version of the current source.

```
1 #include "app.h"
2
3 static uint8_t r_trimming_b[ ] = {4, 5, 6, 7, 8, 9};
4 static uint8_t r_current_sink_b[ ] = {10, 11, 12, 13, 14, 15, 16,
     17};
5 static uint8_t r_current_source_b[ ] = {18, 19, 20, 21, 22, 23,
     24, 25};
6 static uint8_t r_EN_drain = 26;
7 static uint8_t r_EN_source = 27;
8 static uint8_t r_bit_test = 28;
```

9.3 PCB for the Second Version of the Current Source

A new PCB was designed for the second version of the current source. It is used to mount a 3M QFN socket with 80 positions [39] (shown in Figure 9 in subsubsection 2.2.1.2).

It was designed using Autodesk Eagle version 9.6.2. The schematic and board are shown in Figure 69 and Figure 70, respectively. Two pieces of the two-layer PCB were manufactured to use for the measurement process.

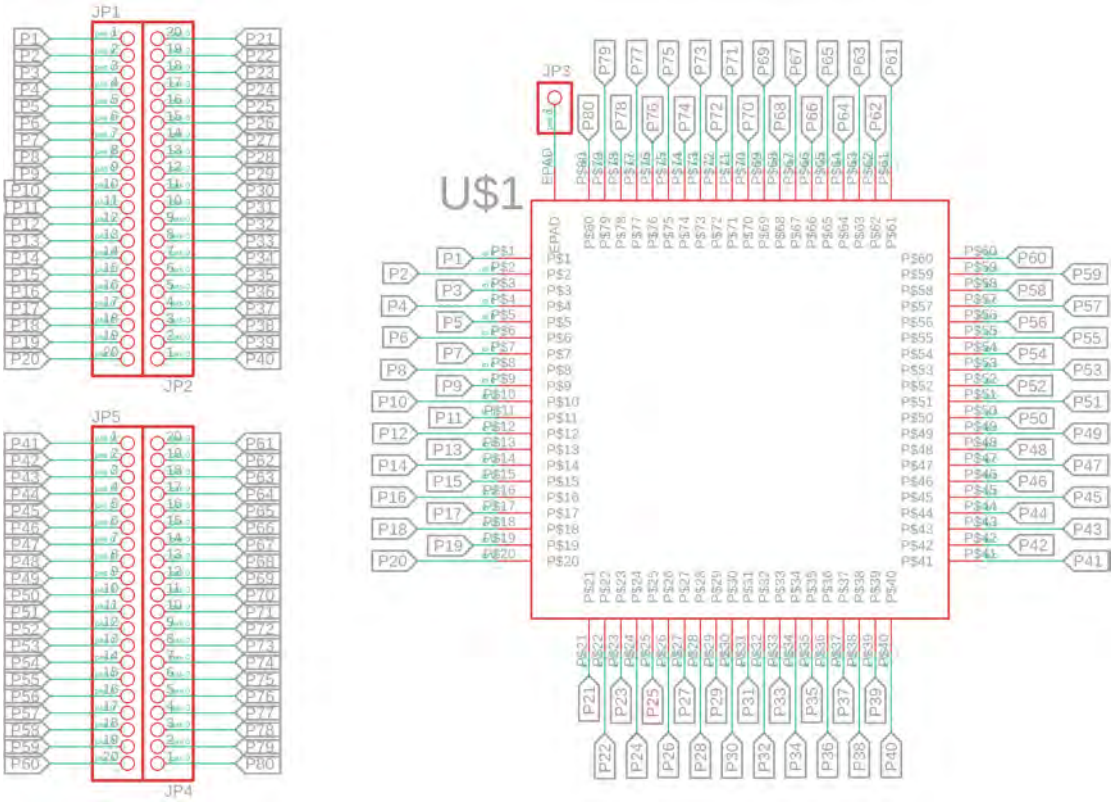

Figure 69: Schematic of the PCB for the socket of version 2 of the current source

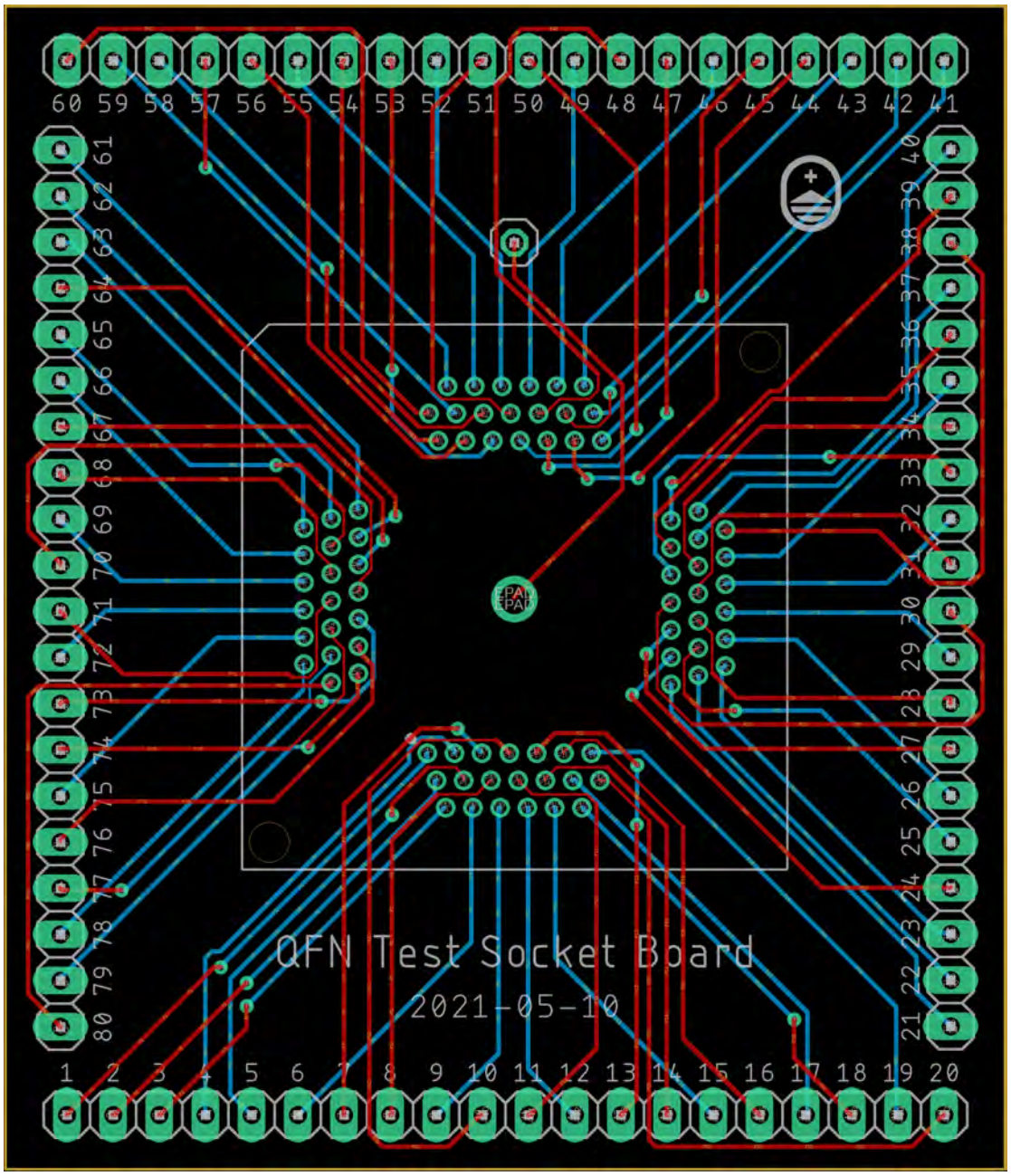

Figure 70: Board of the PCB for the socket of version 2 of the current source

9.4 Design of the Current Sources' Trimming Mechanism

In this section, an overview of the current sources' trimming mechanism is presented.

9.4.1 First version

The design of the first version of the current source is based on the simplified scheme of Figure 71. The basic current source unit has 3 main components: an Operational Transconductance Amplifier (OTA), a valve transistor (M) and a resistance (Rs).

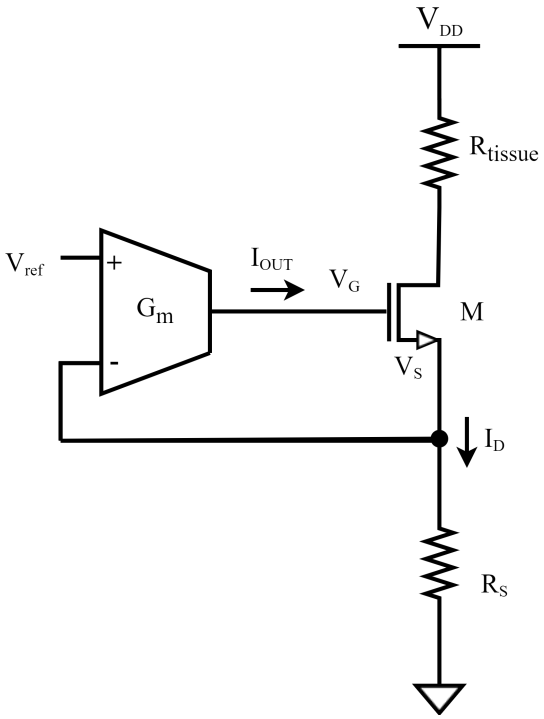

Figure 71: Schematic of the basic current unit for the first version of the current source (from Reference [21]).

The OTA has a high impedance input and an output current (I_{out}) that is ideally a linear function of the differential input voltage ($V_+ - V_-$) as indicated in Equation 30.

$$I_{out} = g_m(V_+ - V_-) \tag{30}$$

The OTA is used in a negative feedback configuration to implement a control loop that forces $V_s = V_{ref}$ and a constant current $I_d = I_{tissue}$ with a value given by Equation 31.

$$I_d = \frac{V_{ref}}{R_s} \tag{31}$$

The detailed characteristics of the design and its behavior are presented in Reference [21].

Multiple branches of this design are implemented to program the different current levels. This is done by attaching or detaching each branch from the circuit using switches controlled by the programming bits.

Since the current on each branch (I_d) is dependent on the reference voltage V_{ref} (Equation 31), changing this voltage will thus change the output current. This is the working principle behind the trimming mechanism.

The V_{ref} voltage is implemented as shown in Figure 72. Here, the trimming bits control which resistors are short-circuited to generate the voltage drop given the current reference I_{ref}. The fine-tuning system is designed such that the minimum change produced in the output current is of around 1%.

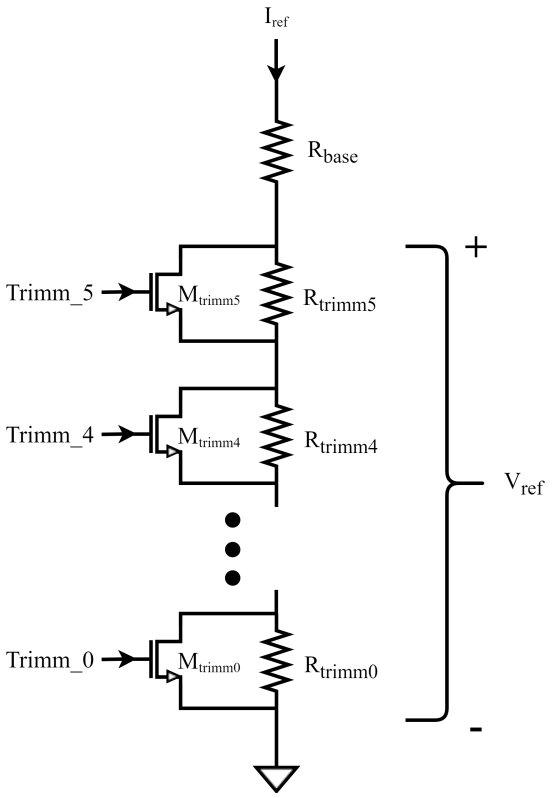

Figure 72: Schematic of the trimming mechanism of the first version of the current source (from Reference [21]).

9.4.2 Second version

A similar design is implemented for the second version of the current source as shown in Figure 73. Here, a single OTA and valve transistor (M) are used. In order to generate the multiple values for the output current, a set of transistors in parallel ($M_0 - M_7$) is incorporated in place of the R_s resistance used in the previous version. The activation of these transistors is controlled by the programming bits ($b_0 - b_7$).

The OTA and valve transistor fix the drain voltage of the NMOS transistors

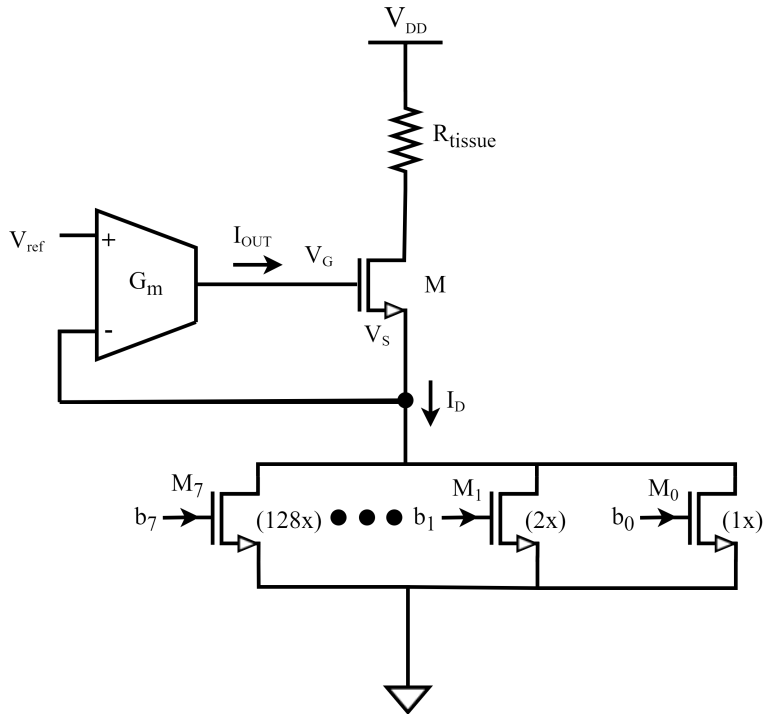

Figure 73: Schematic of the basic current unit for the second version of the current source (from Reference [20]). The numbers shown to the side of transistors M_0 through M_7 indicate the value of the multiplier.

$M_0 - M_7$ to V_{ref} through the control loop. The source voltage V_S is also fixed as it is connected to ground. Hence, the drain-source current through each transistor can be controlled by varying the gate voltage V_G. Given that each branch has a transistor with a multiplier that is twice that of the previous branch, the current through each branch is doubled to obtain the appropriate steps.

To implement the trimming mechanism in this version, V_{ref} is held constant and the voltage V_G is modified. This voltage is generated indirectly by a variable current I_{Gref} which is obtained through a current mirror with multiple branches activated by the trimming bits.

The detailed characteristics of this design and its behavior are presented in Reference [20].