# A Self-biased Current Source, using an Asymmetric Bulk-modified MOS Composite Transistor

Diego Costa
*Departamento de Ingenieria*
*Universidad Católica del Uruguay*
Montevideo, Uruguay
diego1307@gmail.com

Matías Miguez
*Departamento de Ingenieria*
*Universidad Católica del Uruguay*
Montevideo, Uruguay
mmiguez@ucu.edu.uy

Joel Gak
*Departamento de Ingenieria*
*Universidad Católica del Uruguay*
Montevideo, Uruguay
jgak@ucu.edu.uy

Fabián Torres
*Departamento de Ingenieria*
*Universidad Católica del Uruguay*
Montevideo, Uruguay
fabian.torres@correo.ucu.edu.uy

Alfredo Arnaud
*Departamento de Ingenieria*
*Universidad Católica del Uruguay*
Montevideo, Uruguay
aarnaud@ucu.edu.uy

***Abstract*— In this work a new topology for a self-biased current reference, based on an asymmetric bulk-modified MOS (ABM) composite transistor is presented. Two current references based in this technique were designed: a 13.5nA current reference in a 1.5µm CMOS technology, and a 100nA current reference in a 0.18µm CMOS technology. The latter was designed to minimize the temperature dependence of the output current; the result was less than 5% from 0°C to 100°C, which is a very good result in comparison to other reported similar current references.**

***Keywords— Current Mirror, Self-biased Current Source, Low Power, PVT variations, ABM***

## I. INTRODUCTION

A bulk-linearization technique was presented in [1] to enhance the linearity of the MOS transistor, using two series MOSFETs like in Fig. 1; later in [2] this composite structure was examined as a new composite transistor. In Fig. 1 two transistors are connected as a MOS divider to bias the bulk of the self-transistors, defining the equivalent transistor $M_{eq}$ with its own Source (S), Gate (G), Drain (D) terminals; the equivalent bulk terminal is not defined for $M_{eq}$. As pointed in [1], [2], $M_{eq}$ shows an enhanced linear region, where the best results are obtained when the aspect ratios $(W/L)_a$ of $M_a$ and $(W/L)_b$ of $M_b$ are very different $(W/L)_a >> (W/L)_b$. Depending on the transistors' sizes, the resulting composite structure is linear up to an equivalent saturation $V_{Sat\_eq}$ voltage of a few hundred mV like in Fig. 1. Because $(W/L)_a \neq (W/L)_b$ the new composite transistor will be denoted as an asymmetrical bulk-modified transistor or ABM-MOS, and allows to build basic structures like differential pairs or current mirrors [2], to emulate large resistors [1], or exploiting its behavior to implement basic building blocks with a transfer function otherwise difficult to obtain, enabling a new family of circuits. In this work, a simple self-biased current reference in CMOS technology is presented, based in the characteristics of an ABM composite transistor. Firstly, a current mirror where the copy factor *K,*

$$K = I_{Out}/I_{In} \quad (1)$$

depends on the input current $K=K(I_{In})$ is presented, based in an ABM transistor copying to a standard one or vice versa. Then, this non-uniform mirror is utilized to set the operating point of a self-biased current reference. Finally, the design of a $13.5nA_{(nom)}$ and a $100nA_{(nom)}$ current references are shown. The latter was designed to minimize the current dependence on the temperature, achieving only a 5% variation from 0°C to 100°C. Although the proposed new type of current source is not particularly suitable for low voltage operation because of the relatively large saturation voltage of the ABM, and the need of cascode transistors to enhance the mirror's output impedance, it has many parameters to adjust making possible to minimize the current dependence with PVT variations.

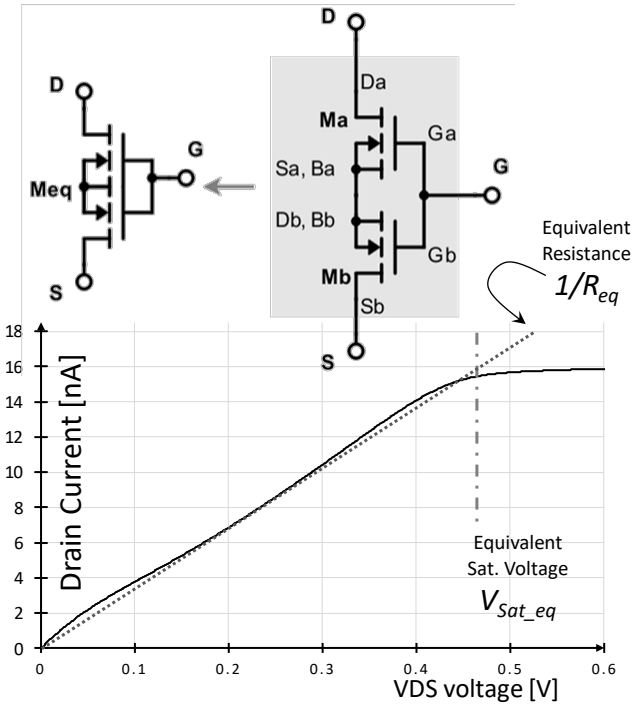
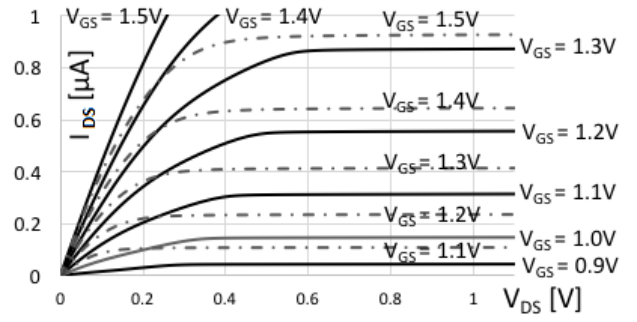
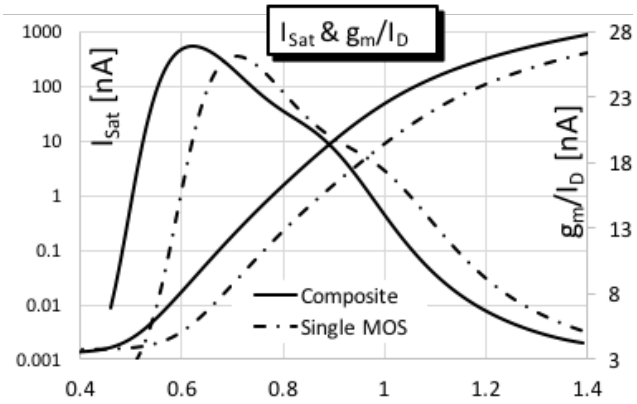


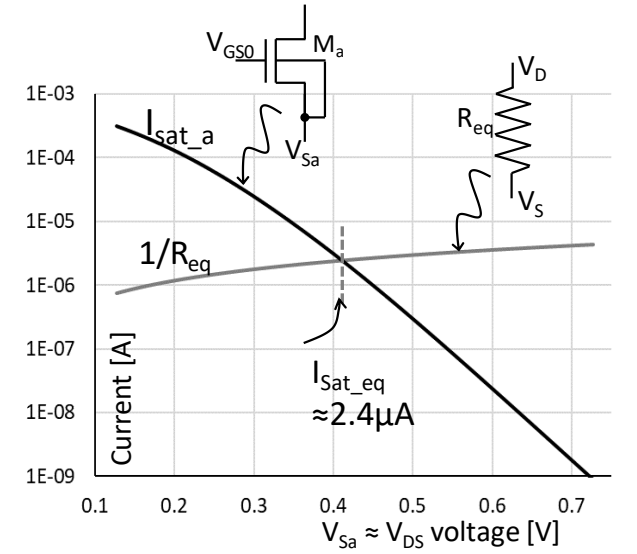

Fig. 1. The ABM-MOS composite transistor. Two MOS transistors $M_a$, $M_b$, are connected in series sharing the bulk terminal to the middle point. In this work the symbol on the left $M_{eq}$ or the explicit composite MOS schematic on the right will be used interchangeably. At the bottom, a simulated curve $I_D(V_{DS})$ is shown for a $W_a/L_a$ = 10µm/0.6µm, $W_b/L_b$ = 0.6µm/40µm ABM-$M_{eq}$, $V_{GS}$ = 1.05V ≈ $V_T$.




(a)




(b)




(c)

Fig. 2. Simulated $I_D(V_{DS})$ for different $V_{GS}$ values in (a), saturation current $I_{Sat}$ and $g_m/I_D$ ratio in (b) and an equivalent saturation of the ABM-MOS estimation using a graphical method in (c). The ABM transistor (continuous line) sizing is $W_a/L_a$ = 10µm/0.6µm, $W_b/L_b$ = 0.6µm/10µm, and a standard n-MOS (dash-dot line) $M_{Ref}$ = 0.6µm/10µm.

## II. THE ABM CURRENT MIRROR

While for the large signal ABM it is not straightforward to develop an analytic expression for the drain current of $M_{eq}$, $I_D(V_{Geq}, V_{Seq}, V_{Deq})$, the design space can be firstly explored with a SPICE simulator. The result for a composite transistor using isolated n-MOS (threshold voltage $V_{TN} \approx 1$V) are presented in Fig. 1 and also in Fig. 2, showing the extended linear range and 'saturation' effects as described in [1],[2]. In Fig. 2b the saturation current $I_{Sat\_eq}(V_{GS})$ and the equivalent $(g_m/I_D)$ ratio [3] are shown for a specific ABM-$M_{eq}$ (continuous lines), in comparison to a single reference transistor $M_{Ref}$ with the bulk connected to the source (dash-dot lines). A quick look to the first two plots in Fig. 2 concludes the ABM behaves approximately as a transistor with an equivalent lower threshold voltage $V_{Teq}$. Apart from the simulated results in Fig.2b, the saturation current of the $M_{eq}$, can be estimated like in Fig. 2c, noting the upper $M_a$ in Fig. 1 always operate with the bulk connected to its source. First the saturation current of a single $M_a$ is simulated (or calculated) for a fixed $V_G$ while varying $V_{Sa}$; then assuming that for the ABM in the linear region $V_{Sa}$ is close to $V_D$ of $M_{eq}$ [1], $V_{Sat\_eq}$ can be calculated intersecting this curve with the linear approach $I_D = V_{DS}/R_{eq}$, where $R_{eq}$ is the equivalent resistance of the ABM in the linear region ([1], see Fig.1). $R_{eq}$ can be estimated with a small signal analysis on $M_b$ at $V_D = 0$. An analytical expression can be derived for example for a relative low drain current assuming, as is reasonable, that $M_a$ is in weak inversion (WI) since $(W/L)_a >> (W/L)_b$ :

$$I_{Sat_{eq}} \approx V_{Sat_{eq}}/R_{eq} = I_{Sa} \cdot e^{\frac{V_G - nV_{Sat_{eq}} - V_T}{nU_T}} \qquad (2)$$

In (2) $V_{Sa}$, $I_{Sa}$, $V_T$, are $M_a$'s source voltage, specific current, and threshold voltage respectively, and $n \approx 1 \cdots 1.5$ is the slope factor. Because of the pseudo saturation effect of $M_{eq}$, apart from pseudo-resistors like in [1], the composite transistor can be utilized to implement operative circuit blocks like current mirrors and differential pairs. An interesting non-standard current mirror is shown in Fig. 3a where the input transistor is a regular p-MOS, and the output transistor is an ABM one. The main difference with a standard current mirror is that the copy factor $K_P$ of (1) is not a constant value regardless the value of $I_{In}$. In the case of the ABM in Fig. 3a, it is necessary to solve (2) to find $I_{Out} = I_{Sat\_eq}$ but the result clearly is not proportional to the input current $I_{In}$; this fact can be also corroborated in Fig.2b. Thus, for the ABM current mirror, $K_P = K_P(I_{In})$, the copy factor is not constant but variable. If the transistors are properly sized, it is possible to achieve a monotonically decreasing function $K_P(I_{In})$ in a range of several orders of magnitude for $I_{In}$.

In Fig. 3b three copy factor curves $K_P(I_{In})$ for a p-MOS ABM mirror are shown for different $M_1$ channel width. Note that for higher $I_{In}$ values $K_P$ is less sensible to changes on the input current. A horizontal line was also included for an arbitrary $K_P$ = 2 showing the intersection points with the previous $K_P(I_{In})$ curves, this intersection will be used in the next section to set the bias point of a current source. There are endless possibilities varying the transistors' size for the ABM mirror curves and horizontal intersection, thus the design space is large (even the ABM mirror can be flipped using the composite transistor at the

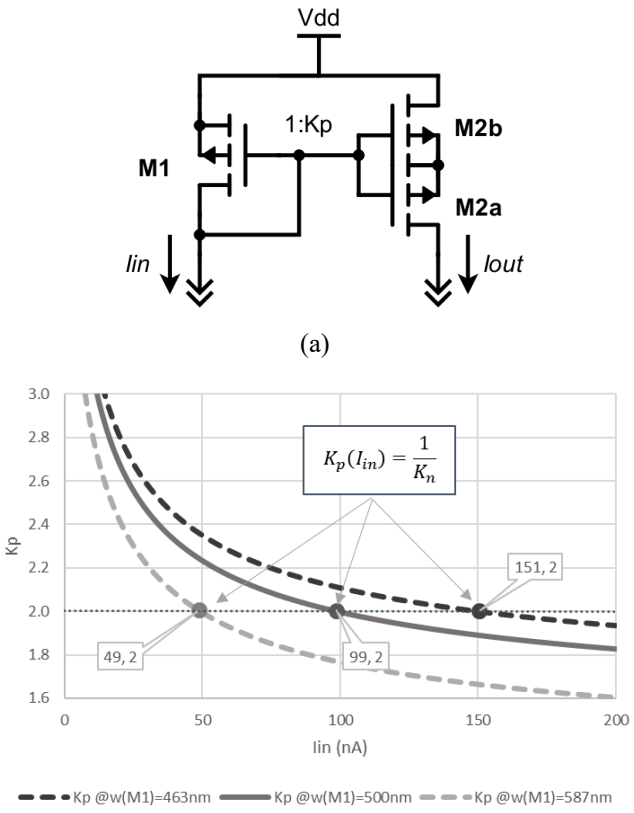



Fig. 3. (a) The ABM current mirror using a regular p-MOS transistor $M_1$ and a p-MOS ABM transistor ($M_{2a}$ - $M_{2b}$). (b) Transfer functions $K_P = K_P(I_{In})$ simulated for three different $M_1$ widths.

input). In the case of Fig. 3b, for $K_P$=2 and $I_{In}$=100nA the transistors are sized: $(W/L)_1$ = 0.5µm/10.5µm, $(W/L)_{2a}$ = 38µm/0.5µm, $(W/L)_{2b}$ = 0.5µm/10µm in a 0.18 µm CMOS technology.

## III. A SELF-BIASED CURRENT SOURCE

The proposed current source is shown in Fig. 4; it is composed by an upper p-MOS ABM current mirror $M_1$-$M_2$ with a non-uniform copy factor $K_P$, and a lower n-MOS standard current mirror $M_6$-$M_5$ with a constant copy factor $K_N$. Additionally, an output mirror $M_6$-$M_8$ with a copy factor $K_{out}$ is included to derive the output current $I_{out}$, and cascode transistors $M_3$-$M_4$-$M_7$ are used to better decouple the effect of the mirrors' output impedance. The input current $I_2$ of the lower mirror is the output of the ABM mirror $I_1$ and vice versa. Therefore, assuming the circuit is stable and converges at a certain current value $I_1$, $I_2$, the operating point will be defined by the following equation in which $K_N$ is a constant and $K_P$ is not.

$$K_P(I_1) = 1/K_N\ ; \tag{3a}$$

$$I_{Out} = K_{Out} \cdot I_1 \tag{3b}$$

The idea is the same behind other self-biased current sources: an upper(lower) constant current mirror and a lower (upper) non-uniform mirror converge to a single bias point. In

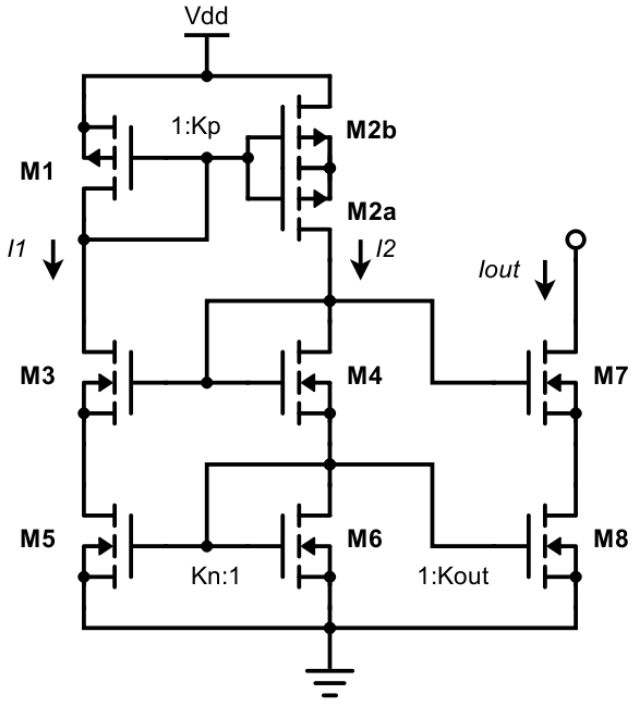
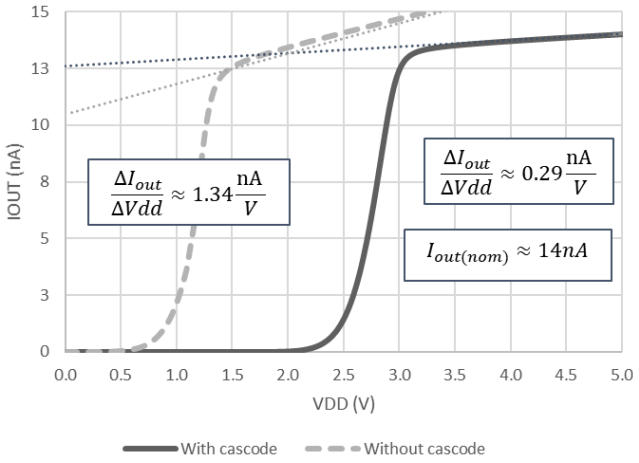


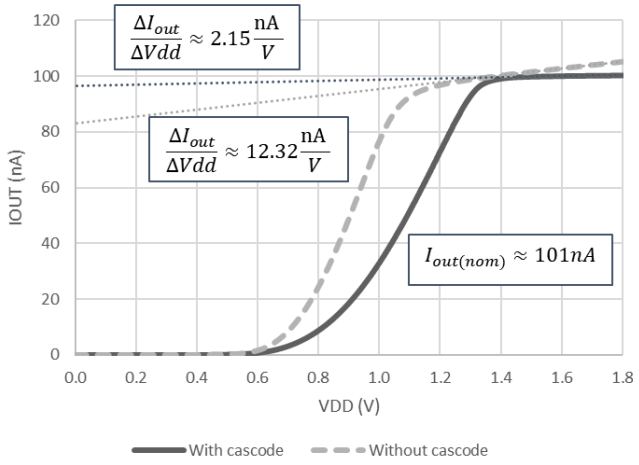

Fig. 4. The ABM-MOS Current Source. The proposed circuit is composed of three distinctive blocks, an upper ABM-MOS current mirror (M1, M2a and M2b), a bottom n-MOS current mirror (M5, M6 and M8) and cascode transistors (M3, M4 and M).

the case of classic BJT bandgaps [4] the non-uniform mirror is a pair of bipolar transistors and a resistor, or the self-cascode MOS (SCM) is used in the case of [5]. Equation (3a) can be graphically solved like in Fig. 3b by the intersection of $K_P(I_1)$ with the horizontal $1/K_N$, and the designer could set the convergence point just by adjusting either the $K_N$ ratio or by tuning the $K_P(I_1)$ curve by changing the ABM mirror's transistors sizes. For example, to design a current source $I_{out}$ of 100nA, assuming $K_N = K_{out}$, from Fig.2b $K_P$ must be intersected at $1/K_N = 2$ so the lower mirror has a ratio $K_N = 0.5$. Two current sources were designed using the proposed topology in two different technologies, in both cases it is arbitrarily assumed that the output current $I_{out} = I_1$. The first one is a $I_{out1}$ = 14nA(nom) current source in a 1.5µm UHV-CMOS technology, using low voltage transistors ($V_{DSmax}$ = 5.5V, $V_{TN}$ = 0.9V, $V_{TP}$ =-0.9V); the second one is a $I_{out2}$ = 100nA(nom) current source in a 0.18µm HV-CMOS technology, using low voltage transistors ($V_{DSmax}$ = 1.9V, $V_{TN}$ = 0.53V, $V_{TP}$ = -0.7V). The DC simulation of both current sources are shown in Fig. 5a and Fig. 5b, and the transistors' sizes are shown in Table I. Two plots are included: with and without the cascode $M_3$-$M_4$, showing its importance to reduce the $V_{dd}$ dependence. In the case of the second current source, it utilizes the ABM mirror of Fig. 3b thus a $K_{N2}$ = 0.5 ratio was selected. The convergence value of $I_{Out2}$ for a high enough $V_{dd}$ is approximately 100nA as expected from Fig. 3b.

Note in Fig. 5, that a trade-off exists about whether to include the cascode transistors or not; while the introduction of the cascode increased the minimum $V_{dd}$ to 1.4V, it also greatly reduced the $V_{dd}$ dependence of the current source. A summary of the simulated main characteristics of the proposed self-biased




(a)




(b)

Fig. 5. Simulation of both designed ABM-MOS self-biased current sources a) 14nA reference in a 1.5µm CMOS technology. (b) 100nA reference in a 0.18µm. The transistor size chart is presented in Table I.

current sources are presented in Table II (for both CMOS technologies), including corner cases (process variations), temperature variation (0-100°C), and $V_{dd}$ sensitivity.

TABLE I. ABM CURRENT SOURCE TRANSISTOR SIZE CHART

| | | W/L (µm/µm) | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | ***M1*** | ***M2a*** | ***M2b*** | ***M5*** | ***M6*** | ***M8*** | ***M3/M4/M7*** |
| ***0.18µm*** | ***W*** | 0.5 | 38 | 0.5 | 100 | 200 | 100 | 20 |
| | ***L*** | 10.5 | 0.5 | 10 | 4 | 4 | 4 | 1 |
| ***1.5µm*** | ***W*** | 4 | 20 | 2 | 1.2 | 1 | 1 | 1 |
| | ***L*** | 40 | 2 | 10 | 12 | 12 | 12 | 5 |

TABLE II. ABM CURRENT SOURCE DIFFERENET IMPLEMENTATIONS CHARACTERISTICS COMPARISSON

| | Simulated Results | | |
|---|---|---|---|
| | ***1.5um.*** | ***0.18um.*** | ***Unit*** |
| $I_{out(nom@25℃)}$ | 14 | 101 | nA |
| $\frac{\Delta I_{out}}{I_{out}}(process)$ | +/-10% | +/-20% | - |
| $\frac{\Delta I_{out}}{I_{out}}(0 \rightarrow 100℃)$ | <35% | <5% | - |
| $\frac{\Delta I_{out}}{\Delta T}(0 \rightarrow 100℃)$ | 47 | 45 | $\frac{pA}{℃}$ |
| $\frac{\Delta I_{out}}{\Delta Vdd}$ | 0.32 | 2.15 | $\frac{\text{nA}}{V}$ |
| Min. $V_{dd}$ | <4.5 | <1.48 | V |
| Min. Output Voltage | 1.25 | 0.4 | V |
| $1/K_N$ | 1.2 | 2 | - |
| Die Area | 0.0238 | n/a | $mm^2$ |

### *A. An untrimmed current source with a low variation with temperature.*

It should be pointed that the designer has many parameters to adjust in Fig. 4: $K_N$, $K_{out}$, and especially the $K_P$ curve that depends on $M_1$, $M_{2a(b)}$, sizes. Thus, the design space exploration is complex and some design criteria must be chosen. But that many parameters to adjust may allow reducing PVT variations of the nominal current value. The premise for the design of the second current source was to reduce as much as possible, the fluctuations of $I_{out}$ with temperature. The design space exploration was carried via simulator, and for the typical transistor model, varying the temperature $T$ from 0°C to 100°C. First an arbitrarily long $M_1$ transistor was selected, and then a $W_1$ was modified, which shifts $K_P$ to a point where $\Delta I_{Out}$ was at

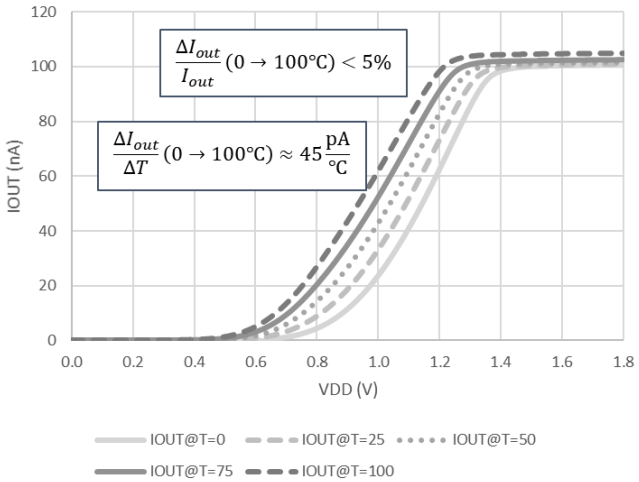



Fig. 6. The source response to a temperature variation from 0°C to 100°C.

its minimum and $1/K_N$ was not impractical. Once $W_1$ was selected the same method was applied for each of the ABM Mirror transistors sizes. Finally, through an iterative process a minimum variation for $I_{out}(T)$ was achieved in the full temperature range.

The nominal current variation shows promising results with $\Delta I_{Out}/I_{Out} < 5\%$, $\Delta I_{Out}/\Delta T = 45pA/°C$, from 0°C to 100°C (these values are reduced to only $\Delta I_{Out}/I_{Out} < 2\%$, $\Delta I_{Out}/\Delta T = 29pA/°C$, from 0°C to 75°C), in comparison to other simple untrimmed reported current sources like [6], [7].

## IV. Conclusions

In this work, a new family of self-biased current references was presented, using an asymmetric bulk-modified MOS (ABM) composite transistor as the key element. The idea is to connect an ABM mirror where the copy factor $K_P$ depends on the copy current, to a standard mirror with a constant copy factor $K_N$. The result is a self-biased current reference circuit converging to a single output reference current $I_{out}$ that depends on the $K_N$, and on the ABM transistor's sizes. Two current references based in the proposed topology were presented: first an $I_{out1}$ = 14nA current source in a 1.5µm CMOS technology, and then an $I_{out2}$ = 100nA current source in a 0.18µm HV-CMOS technology. A summary of the simulated main characteristics of the proposed self-biased current sources are presented in Table II.

The design-space exploration is complex with those many parameters to adjust. Moreover, also the topology can be changed by flipping the ABM mirror placing the composite transistor at the mirror's input branch or using two ABM mirrors instead of a single and a classic one. Since the proposed circuit block is new, there is still a need to set a proper design methodology and design criteria. But it is possible to assume that so many parameters to adjust, may allow finding certain operating points with a reduced impact of PVT variations on $I_{Out}$. The second current source was designed by means of a simulator-driven design-space exploration, to reduce the impact of temperature to a minimum. Without further trimming $I_{out2}$ = 100nA varies less than 5% from 0°C to 100°C, which is a very promising result.

## Acknowledgment

This Project was partially funded by grants FCE_3_2018_1_148263 and POS_NAC_2018_1_151733 by ANII-Uruguay.

## References

[1] A.Arnaud and M.R. Miguez, "Bulk linearisation of the MOS resistor," in *Electron. Lett*., vol.54, no.19, pp. 1106-1108, Sept. 2018.

[2] A. Arnaud, R. Puyol, A. Chacón-Rodríguez, M. Miguez and J. Gak, "An asymmetrical bulk-modified composite MOS transistor with enhanced linearity," in *Proc. IEEE Latin American Symp. on Circuits & Systems, LASCAS'2019*, pp. 49-52, Feb. 2019.

[3] F. Silveira, D. Flandre, and P. G. A. Jespers, "A $g_m/I_D$ based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid State Circuits*, vol.31, no.9, pp.1314-1319, Sept. 1996.

[4] A. Paul Brokaw, "A simple three-terminal IC bandgap reference", *IEEE J. Solid-State Circuits* , vol.9, no.6, pp.388-393, Dec. 1974.

[5] E. M. Camacho-Galeano, C. Galup-Montoro and M. C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 2, pp. 61-65, Feb. 2005.

[6] E.M. Camacho-Galeano, et. al., "Temperature performance of sub-1V ultra-low power current sources," in *Proc. IEEE Int. Symp. on Circuits and Systems*, *ISCAS'2008*, pp.2230-2233, May 2008.

[7] Joan Santamaria, Nestor Cuevas, Luis E. Rueda G., Javier Ardila, and Elkim Roa, "A Family of Compact Trim-Free CMOS Nano-Ampere Current References", in *Proc. IEEE Int. Symp. on Circuits and Systems*, *ISCAS'2019*, May 2019.